Instruction Manual

Tektronix

92DM74
R3000 & R3000A Microprocessor Support

070-8090-00

This manual supports software Release 2,
Version 1.50 and above.

Warning
The servicing instructions are for use by qualified
personnel only. To avoid personal injury, do not
perform any servicing unless you are qualified to
do so. Refer to the Safety Summary prior to
performing service.

**Please check for change information at the rear
of this manual.**

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Preface: A GUIDE TO DAS 9200 DOCUMENTATION

The Digital Analysis System (DAS) 9200 documentation package provides the information necessary to install, operate, maintain, and service the DAS 9200. The DAS 9200 documentation consists of the following:

- a series of microprocessor-specific **microprocessor support instructions** that describe the various microprocessor support packages

- a **system user's manual** that includes a beginning user's orientation, a discussion of DAS 9200 system-level operation, and reference information such as installation procedures, specifications, error messages, and a complete system glossary

- a series of **module user's manuals** that describe each of the DAS 9200 acquisition, pattern generation, and optional I/O modules

- an **on-line documentation** package that includes "context-sensitive" technical notes

- a **programmatic command language user's manual** that describes the set of programmatic commands available for remotely controlling the DAS 9200

- a series of **application software user's manuals** that describe the various application software packages

- a **technician's reference manual** that helps a qualified technician isolate DAS 9200 problems to the individual module level and determine corrective action (including on-site removal and replacement of modules)

- a **verification and adjustment procedures manual** that allows a qualified technician to make necessary adjustments and verify specifications of the mainframe and modules

- a series of **workbooks** that teach concepts about DAS 9200 acquisition modules and pattern generation modules

GENERAL SAFETY SUMMARY

The general safety information in this summary is for operating and servicing personnel. Specific warnings and cautions can be found throughout the manual where they apply, and may not appear in this summary.

TERMS IN THIS MANUAL

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

TERMS AS MARKED ON EQUIPMENT

CAUTION indicates a hazard to property, including the equipment itself, and could cause minor personal injury.

WARNING indicates solely a personal injury hazard not immediately accessible as you read the marking.

DANGER indicates a personal injury hazard immediately accessible as you read the marking.

SYMBOLS AS MARKED ON EQUIPMENT

DANGER—High voltage.

Protective ground (earth) terminal.

ATTENTION—REFER TO MANUAL.

GROUNDING THE PRODUCT

This product is intended to operate from a power source that does not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground.

WARNING: This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle. A protective-ground connection by way of the grounding conductor in the power cord is essential for safe operation. (I.E.C. Safety Class I)

DANGER ARISING FROM LOSS OF GROUND

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulated) can render an electric shock.

POWER DISCONNECT

The main power disconnect is by means of the power cord or, if provided, an ac power switch.

USE THE PROPER POWER CORD

Use only the power cord and connector specified for your product. Use only a power cord that is in good condition. CSA Certification includes the equipment and power cords appropriate for use on the North America power network. All other power cords supplied are approved for the country of use.

USE THE PROPER FUSE

To avoid fire hazard use only a fuse of the correct type, voltage rating, and current rating.

USE THE PROPER VOLTAGE SETTING

Make sure the line selector is in the proper position for the power source being used.

REMOVE LOOSE OBJECTS

During disassembly or installation procedures, screws or other small objects may fall to the bottom of the mainframe. To avoid shorting out the power supply, do not power-up the instrument until such objects have been removed.

DO NOT OPERATE WITHOUT COVERS

To avoid personal injury or damage to the product, do not operate this product with covers or panels removed.

USE CARE WITH COVERS REMOVED

To avoid personal injury, remove jewelry such as rings, watches, and other metallic objects before removing the cover. Do not touch exposed connections and components within the product while the power cord is connected.

REMOVE FROM OPERATION

If you have reason to believe that the instrument has suffered a component failure, do not operate the instrument until the cause of the failure has been determined and corrected.

DO NOT OPERATE IN EXPLOSIVE ATMOSPHERES

To avoid explosion, do not operate this product in an explosive atmosphere unless it has been specifically certified for such operation.

Section 1: OVERVIEW

The 92DM74 Microprocessor Support product disassembles data from systems based on the MIPS R3000 or R3000A RISC microprocessor. The 92DM74 product runs on a DAS 9200 system equipped with a 92A96 Data Acquisition Module.

This product consists of software on a floppy disk, a probe adapter, and this manual. The software includes both setup files and a disassembler program.

Included in the software files are two demonstration reference memory files. One file (called R3000_Demo) shows disassembled data; all figures in Section 4 that show acquired data are taken from this demonstration reference memory. A second reference memory file contains timing information and is discussed in Section 5. In addition to the two reference memory files, there is a module setup file (called R3K_Timg_96) used to set up the DAS 9200 for asynchronous bus analysis as described in Section 5. All of these files are automatically installed on the DAS 9200 when you install the disassembler software.

BASIC INFORMATION

To use this product, you need to have the following:

- this manual
- other DAS 9200 mainframe and data acquisition module user's manuals
- knowledge of your specific DAS 9200 configuration and its operation
- the *mips RISC Architecture* (1988, Prentice Hall), *IDT RISC R3000 Family System Programmer's Guide* (1988, Integrated Device Technology), and *R3000 Family Hardware User Manual* (1988, Integrated Device Technology) or any of the equivalent manuals from the R3000 component vendors
- knowledge of your R3000 system

DAS 9200 System Software Compatibility

The R3000/A application software is compatible with DAS 9200 System Software Release 2, Version 1.5 or greater. It is not compatible with previous versions.

About This Manual

The organization of this manual is based on the sequence of steps necessary to use the disassembler. If you are an experienced DAS 9200 user familiar with loading software and connecting microprocessor support probe adapters to a system under test, you can use the *Quick Start* section. The *Quick Start* section gives brief instructions on how to install the R3000/A software, connect the DAS 9200 to your R3000 system, configure the probe adapter, and acquire data. You can then proceed to either Section 4 or 5 depending on whether you're using disassembly or performing hardware analysis.

If you are using DAS 9200 microprocessor support for the first time, you should read some sections sequentially. Read Sections 1, 3, and 4 if you are going to acquire and view disassembled data. Read Sections 1, 3, and 5 if you are going to acquire and view timing or state data for hardware analysis. Figure 1-1 shows how to proceed through this manual.
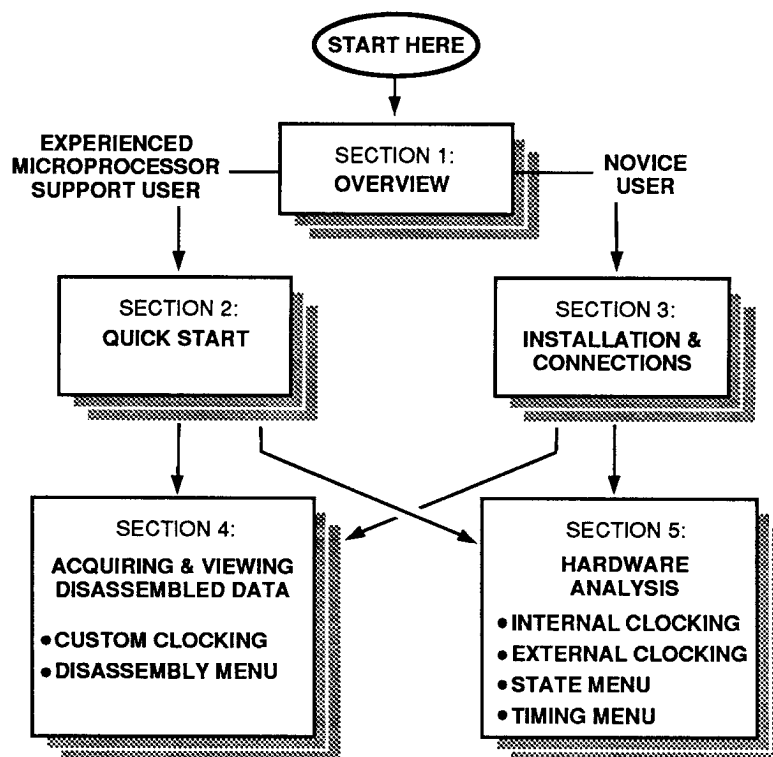
Figure 1-1. How to proceed through this manual.

In this manual, the following conventions are used:

- the terms disassembler and disassembler software are used interchangeably throughout this manual in reference to the software that disassembles the bus cycles into instruction mnemonics and cycle types

- the terms system under test and SUT are used interchangeably when referring to the microprocessor system under test

- references to the 92A96 Data Acquisition Module include all versions of that module unless otherwise noted

- active low signals in this document have an asterisk (*) following the signal name; for example, Reset *

- the term R3000 applies to both R3000 and R3000A systems

Other Necessary Manuals

Before using these instructions, you should be familiar with the operation of a DAS 9200 with the data acquisition module you are using. For general instructions on the use of the DAS 9200 and a data acquisition module, refer to both the *DAS 9200 System User's Manual* and the data acquisition module user's manual.

Refer to the *mips RISC Architecture* (1989, Prentice Hall), *IDT RISC R3000 Family System Programmer's Guide* (1988, Integrated Device Technology), and *R3000 Family Hardware User Manual* (1988, Integrated Device Technology), or equivalent manuals for information about the R3000 microprocessor.

DAS 9200 Configuration

To use the R3000 microprocessor support package, your DAS 9200 must be equipped with at least one 92A96 Data Acquisition Module with probe cables and standard probes.

The standard probe assemblies consist of four sets that have one clock data probe and three 8-channel data probes each. The clock probe (a single channel), and each channel of the 8-channel probe, has one signal connection and one ground connection. Leadsets and grabber tips are not required.

Figure 1-2 shows an overview of the DAS 9200 connected to the system under test.
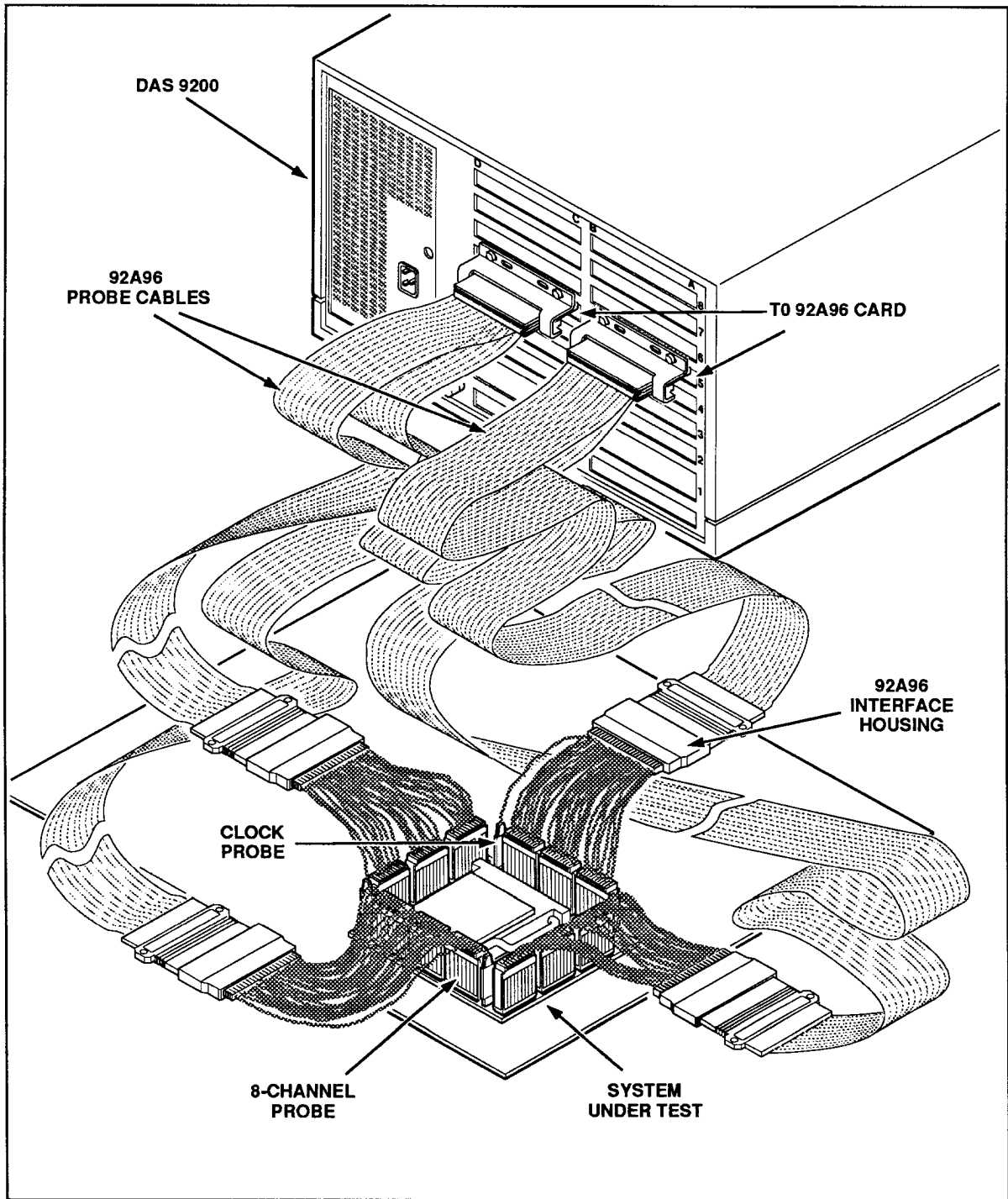
Figure 1-2.   Overview of a DAS 9200 connected to a system under test.

DIFFERENCES BETWEEN THE 92A96 AND 92A60/90 MODULES

If you have used a DAS 9200 with a 92A60/90 Module but haven't used a 92A96 Module, there are some key differences you should note. Table 1-1 lists the key differences.

Table 1-1
Differences Between 92A96 and 92A60/90 Data Acquisition Modules

Characteristic	92A96 Module	92A60/90 Module
Maximum synchronous data sampling rates	100 MHz	20 MHz
Maximum asynchronous data sampling rates	400 MHz, 24 channels or 200 MHz, 48 channels or 100 MHz, 96 channels	20 MHz, 60 or 90 channels
Memory depth	92A96, 8K 92A96D, 32K	92A90, 32K 92A90D, 128K
Physical connections to the probe adapter	4 probe cables, each connecting to 1 clock probe and three 8-channel probes	2 or 3 cables connecting to 1 buffer probe
Clock channels	Not stored as data	Stored as data
Clock Menu selections	Custom, Internal, External	Micro, Demux, Internal, External
Flags	1 flag	2 flags
Counter/timers	2 counter/timers	3 counter/timers
Counter/timer width	32-bit counter/timer	24-bit counter/timer
Word/range recognizers	8 word and 0 range or 6 word and 1 range or 4 word and 2 range	8 word and 2 range

R3000/A SYSTEM REQUIREMENTS AND RESTRICTIONS

You should consider your system requirements and restrictions of the R3000 microprocessor before operating the disassembler. You should also consider all electrical, environmental, and mechanical specifications in Appendix C as they pertain to your system under test. The remainder of this section describes R3000 constraints.

System Clock Rate. The microprocessor support package supports the R3000 microprocessor running up to 33 MHz[1].

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[1] Specification at time of printing. Contact your DAS 9200 sales representative for current information on the fastest devices supported.

Timing Constraints. The 92DM74 supports various speed versions of the R3000 microprocessor. The 92DM74 timing requirements can cause timing constraints that are more restrictive than the microprocessor requirements. In addition, the microprocessor timing specifications vary from vendor to vendor. Refer to *Supplemental Timing Information* in Appendix B for information on the timing constraints of the various speed versions.

Cache Swapping. To facilitate cache invalidation and diagnostics, the R3000 microprocessor can swap the Instruction and Data caches under program control. During the cache swapping operation, the disassembler can lose a few samples or acquire a few invalid samples as it compensates for the cache swapping.

Cache Miss and Branch Detection. The disassembler detects cache misses and determines when branches are taken by scanning adjoining samples in the acquisition memory. The disassembler may not complete the scan when it disassembles samples near the beginning or near the end of the acquisition memory. Qualification gaps, extremely long stalls, or reassertion of the Reset signal can also prevent the disassembler from completing its scan. In such cases, the disassembler will assume that a cache access failed (missed) or a branch was not taken. Also, in such cases, the disassembler can incorrectly calculate the target address of a jump instruction.

Exception Processing. The disassembler monitors a signal from the R3000 CPU that indicates when the start of exception processing has blocked an instruction from executing in the instruction pipeline. The disassembler marks those instructions as Not Executed (unless it is obvious that the instruction caused the exception). You can disassemble instructions labeled (NOT EXECUTED) by using the Mark Data function as described in *Marking Cycles* in Section 4.

R3000 Register Nomenclature. The disassembler can display the names of the CPU's general purpose registers using either software or hardware formats as selected in the Disassembly Format Definition overlay. The disassembler uses F0–31 for the R3010 Floating Point Coprocessor general registers and descriptive names for the various coprocessor control registers. The disassembler makes no attempt to flag illegal register usage (such as specifying odd-numbered registers for floating point operations).

Byte Ordering. The disassembler uses either Big-Endian or Little-Endian memory byte ordering for instruction disassembly depending on the position of the Big/Little jumper on the probe adapter. Depending on your system's requirements, you should set this jumper to the correct position before acquiring data. You can also override the jumper position while in the Disassembly menu (refer to the *Disassembly Format Definition Overlay* in Section 4).

Probe Adapter Clearance. Your R3000 system must have a minimum amount of horizontal and vertical clearance surrounding the R3000 microprocessor to accommodate either the standard or optional probe adapter. Figures C-1 and C-2 in *Appendix C: Service Information* show these dimensions.

R3000 System and Probe Adapter Cooling. You must be sure to retain the original level of cooling for your R3000 system after you install the probe adapter. To maintain the required operating temperature, you may be required to provide additional cooling for the probe adapter.

Probe Loading. Any electrical connection to your system adds an additional ac and dc load. The 92A96 probes and R3000 probe adapter were carefully designed to add the minimum possible load to your system. This additional load may affect the operation of the R3000 system in systems with extremely tight timing margins. Appendix C contains complete specifications on how the R3000 probe adapter affects your system.

Pin Alignment. Because of the low profile design of the probe adapter, it is easy to misalign the probe adapter when placing it in the system under test and can damage the microprocessor, probe adapter, or the system under test. It is important to verify the proper pin alignment prior to applying power to the system under test.

Section 2: QUICK START

If you are an experienced user of a 92A60, 92A90, or 92A96 Data Acquisition Module, you can use this section to quickly set up your system and use it. Before setting up your system, read the discussion on *R3000/A System Requirements and Restrictions* in Section 1.

If you have more than one 92A96 Module in the DAS 9200, you should apply slot number labels to various parts of the DAS 9200 equipment. Refer to the discussion on *Labels* in Section 3 for a description of where to apply the slot number labels. These slot numbers will help you identify which 92A96 Module is connected to the probe adapter in a multimodule system.

A Symbol table is presented at the end of this Section for you to remove or photocopy. This provides you with an easy reference when setting up the Trigger menu using symbols. The symbol table is duplicated in Section 3 in case it is lost or damaged after being removed.

The probe adapter is shipped with a 145-pin replaceable protective socket installed in addition to a 175-pin socket. If your R3000 system uses the R3000A microprocessor, you need to replace the 145-pin socket with the 175-pin socket. Refer to *Removing and Replacing Sockets* in Appendix C for instructions on replacing the protective sockets.

INSTALLING SOFTWARE

To install the R3000 support software, follow these steps:

1. Power on the DAS 9200 and select the Disk Services menu.
2. Select Install Application and press F8: EXECUTE OPERATION.
3. Follow the on-screen prompts.

You may need to remove applications or files from the hard disk if there is not enough available disk free space to accommodate the microprocessor support files.

CONFIGURING THE PROBE ADAPTER

The R3000 probe adapter has two user-configurable jumpers that must be configured before you acquire data the first time.

The Big/Little Endian jumper lets you select the byte ordering: Big-Endian or Little-Endian. Determine which byte ordering is required by your system and set the jumper accordingly. The jumper is shipped in the Big-Endian position.

The Timing/Normal jumper lets you configure the disassembler to run in Timing (Transparent) mode. The Timing mode bypasses the additional latching or stretching of selected signals on the probe adapter. Signals that are buffered or latched in the Normal mode are buffered in the Timing mode. For Disassembly purposes, you should leave the jumper in the Normal position. Determine whether or not you need to run in Transparent mode and set the jumpers accordingly.

CONNECTING THE DAS 9200 TO THE R3000 SYSTEM

To connect the 92A96 Module clocks and 8-channel probes to the probe adapter, follow this procedure:

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CAUTION
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Static discharge can damage the microprocessor, 8-channel probes, clock probes, or the 92A96 Module. To prevent static damage, observe the following precautions while following all connection procedures.

Handle the microprocessor only in a static-free environment.

Always wear a grounding wrist strap, or similar device, while handling the microprocessor and probe adapter.

Discharge stored static electricity from the probe adapter by touching any of the ground pins (the row of pins closest to the edge of the probe adapter circuit board).

1. Use the antistatic shipping material to support the probe adapter while connecting the clock and 8-channel probes as shown in Figure 2-1. This prevents the circuit board from being flexed and the socket pins from being bent.

Hold the 8-Channel probes by the podlet holder when connecting them to the probe adapter. Do not hold them by the cables or neck of the podlets.
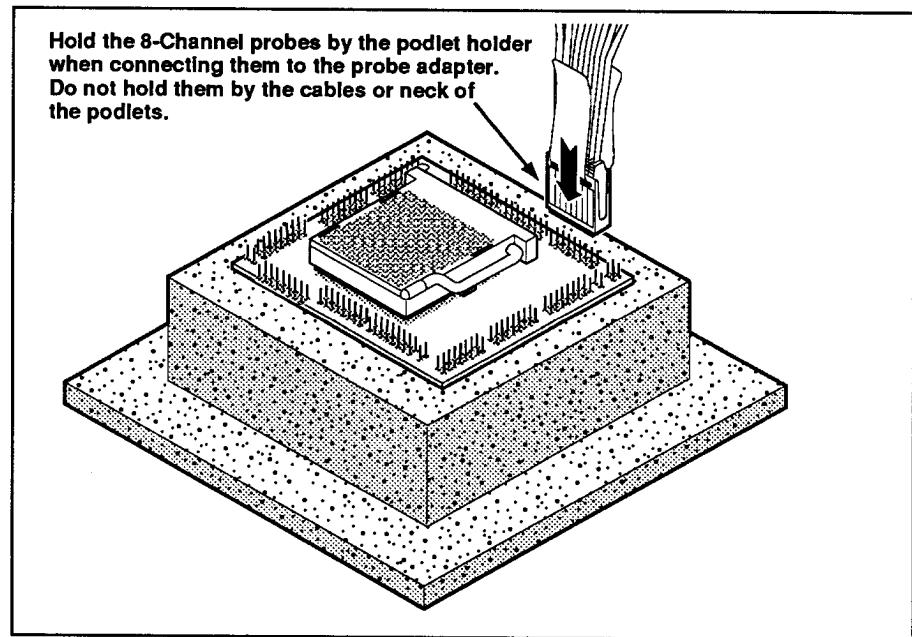
Figure 2-1. Connecting the probes to the probe adapter.

2. Match the Section names and channel numbers on the interface housing to the probe adapter.

> **CAUTION**
>
> *Connect only the signal connectors to the signal pins and the ground connectors to the ground pins. Connecting any R3000 signal to a probe adapter ground pin can damage the microprocessor or the probe adapter circuitry.*

3. Connect the clocks and 8-channel probes to the appropriate sets of square pins on the probe adapter as shown in Figure 2-2. The signal connector is on the color-coded side of the podlet; the ground connector is on the opposite side of the podlet.

> *NOTE*
>
> *If your podlets are not installed in a podlet holder, or are not installed in the proper order, refer to* Removing and Replacing Podlets *in Appendix C.*

4. Power down your R3000 system and carefully remove the microprocessor. (It is not necessary to power down the DAS 9200.)
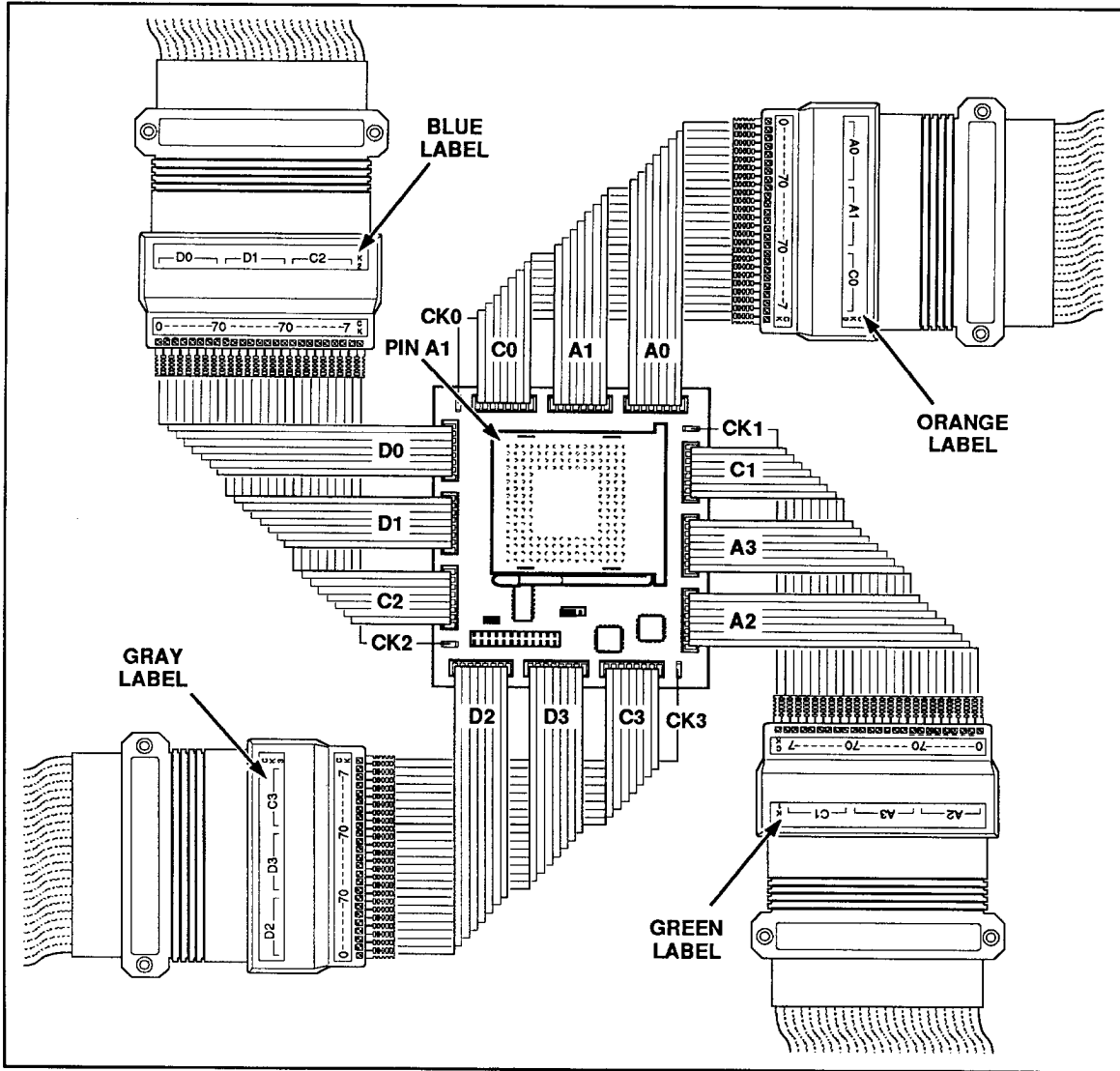
Figure 2-2. Connections from the 92A96 probe cables to the probe adapter.

```
........................
:     CAUTION          :
........................
```

*The microprocessor can be permanently
damaged if you insert it improperly on the probe
adapter. Pin A1 on the microprocessor must
align with pin A1 on the ZIF socket of the probe
adapter.*

*Offsetting the probe adapter by one row of pins
on the SUT can damage the microprocessor,
probe adapter, or SUT. The probe adapter must
align with pin A1 of the SUT. See Figure 2-3 for
proper alignment of pin A1 on the
microprocessor, the ZIF socket, and the R3000
system socket.*

5. Refer to Figure 2-3 and carefully plug the probe adapter
into the R3000 system socket. Align pin A1 on the probe
adapter to pin A1 on the R3000 system socket.
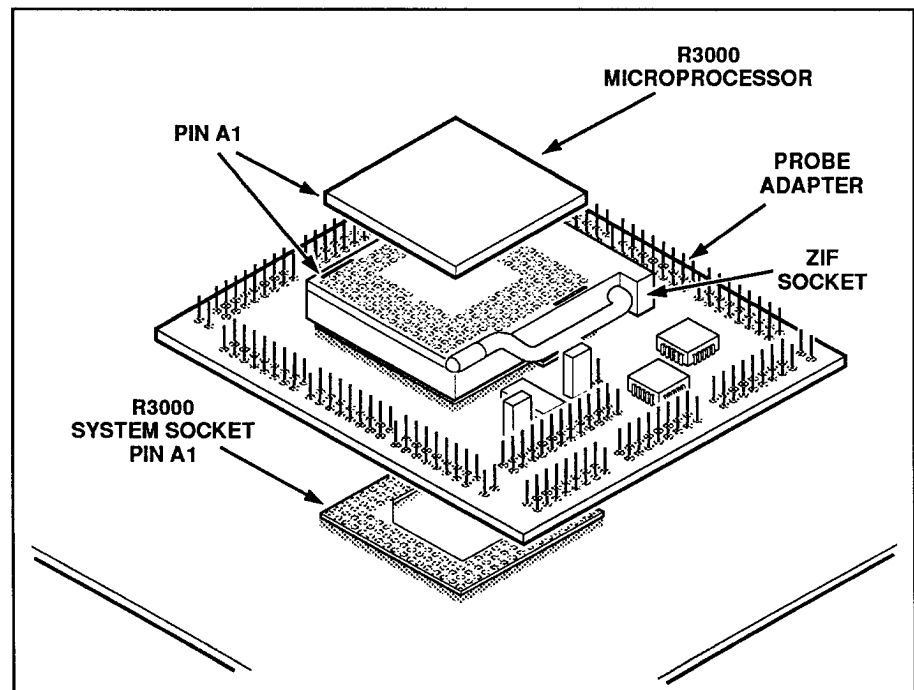
Figure 2-3. Placing the probe adapter in the R3000 system.

NOTE

If your system under test has a ZIF socket with a lever attached, you might need to remove the protective socket from the bottom of the probe adapter, place it in your system's ZIF socket, close the ZIF socket, and install the probe adapter in the protective socket. Refer to Removing and Replacing Sockets *in Appendix C for information on removing the protective sockets from the probe adapter.*

6. Open the ZIF socket by pulling the lever up and away from the socket.

7. Carefully plug the microprocessor into the ZIF socket. Align pin A1 on the microprocessor to pin A1 of the socket.

8. Push the ZIF socket's lever down to lock the ZIF socket.

If the 92A96 Module probe cables are not already connected to the interface housings, refer to Figure 2-2 and follow this procedure:

1. Match the color of the label on the interface housing to the color of the label on the loose end of a 92A96 probe cable.

2. Line up the key and key slot and connect them.

3. Repeat steps 1 and 2 for the other three interface housings and probe cables.

SETTING UP THE DISASSEMBLER

The 92DM74 software is designed to work with a single 92A96 Module only. If your DAS 9200 contains more than one 92A96 Module, you will have to use the System Configuration menu to reconfigure the 92A96 Modules into singlecard modules prior to setting up the disassembler.

To set up the disassembler, perform the following steps:

1. Access the Configuration menu and select R3000 Support in the Software Support field. When you do this, the Channel, Clock, and Trigger menus will be set up for microprocessor support.

NOTE

Remember to read the discussion R3000 System Requirements and Restrictions *in Section 1 prior to setting up the 92A96 Module for disassembly.*

Do not disturb the Address, Data, Jumper, or Control groups (in the Channel menu) or the channel assignments within them while using the disassembler. Changing these groups causes invalid instruction mnemonics disassembly. You can find the channel group definitions and channel assignments in Appendix C.

2. Refer to the Clock menu and set up your Custom clocking choices. Refer to Appendix B for details on the clocking selections available with the Custom clocking menu.

3. If you are performing hardware analysis, you can select Internal or External clocking in the Clock menu. Mnemonic disassembly and the Control group Symbol Table labels can be invalid with either of these clocking modes.

4. The default trigger program will trigger on the first data sample acquired after pressing F1: START. Select the Trigger menu if you want to change the trigger program.

Table 2-1 is a Control group symbol table intended for you to remove or photocopy and use while performing disassembly. Refer to Section 4 for information on displaying the Control group with the Disassembly menu.

ACQUIRING AND DISPLAYING DATA

After completing the DAS 9200 and probe adapter setups, you can acquire and display data. Perform the following steps:

1. Power on the R3000 system under test.

2. Press F1: START.

   After satisfying the trigger program and filling acquisition memory, the DAS 9200 will display data in the default State menu.

3. Select the Disasm menu from the Menu Selection overlay to view disassembled data.

4. Select the State menu or the Timing menu from the Menu Selection overlay to view data for hardware or timing analysis. (Note that the probe adapter circuitry latches and stretches some signals to help the disassembly unless the Timing/Normal jumper is placed in the Timing position.)

The Disassembly menu displays the disassembled data in different formats:

- Hardware format shows instruction mnemonics on Fetch cycles and cycle-type information for all other cycles.

- Software format shows only opcode fetches; all other cycle types are suppressed.

- Control Flow format shows only instructions that change the control flow.

- Subroutine format shows only subroutine calls, exceptions, and returns.

Refer to *Appendix A: Error Messages and Disassembly Problems* if you have problems acquiring and displaying data.

This is the end of the *Quick Start* section.

Table 2-1
Control Group Symbol Table (R3000_Ctrl)

Symbol	Run*	Phase	Exc*	XEn*	IRd*	IWr*	DRd*	DWr*	MemRd*	MemWr*	RdBusy	WrBusy*	Reset*	AccTyp2	AccTyp1	AccTyp0	Meaning
INSTR_STREAMING	0	1	X	0	X	X	X	X	X	X	X	X	1	X	X	X	Instruction fetched during streaming
SWAPPED_INST_RUN	0	1	X	X	X	X	0	X	X	X	X	X	1	X	X	X	Swapped Instruction run cycle
INST_RUN/EXC1W	0	1	0	X	X	X	X	X	X	X	X	X	1	X	X	X	Exception indication Exc1W†
INST_RUN	0	1	X	X	X	X	X	X	X	X	X	X	1	X	X	X	Instruction Phase of a run cycle
INST_STALL/RETRY	1	1	X	0	X	X	X	X	X	X	1	X	1	X	X	X	Instruction Phase of a Stall, read with Retry
INST_FIXUP/READ	1	1	0	0	X	X	X	X	X	X	X	X	1	X	X	X	Instruction Read from main memory during a Fixup cycle
INST_REFILL	1	1	1	0	X	X	X	X	X	X	X	X	1	X	X	X	Instruction Phase of a Refill cycle
INST_FIXUP	1	1	0	X	X	X	X	X	X	X	X	X	1	X	X	X	Instruction Phase of a Fixup cycle‡
INST_STALL	1	1	1	X	X	X	X	X	X	X	X	X	1	X	X	X	Instruction Phase of a Stall cycle‡
UNCACHED_INST	X	1	X	0	X	1	X	1	X	X	X	X	1	X	X	X	Any uncached Instruction fetch
MAIN_MEM_INST_READ	X	1	X	0	X	X	X	X	X	X	X	X	1	X	X	X	Read instruction from main memory
DATA_RUN/RD_BYTE	0	0	X	X	X	X	0	X	X	X	X	X	1	0	0	0	Data Phase run cycle single-byte read
DATA_RUN/RD_2-BYTE	0	0	X	X	X	X	0	X	X	X	X	X	1	0	0	1	Data Phase run cycle half word read
DATA_RUN/RD_3-BYTE	0	0	X	X	X	X	0	X	X	X	X	X	1	0	1	0	Data Phase run cycle tribyte read
DATA_RUN/RD_WORD	0	0	X	X	X	X	0	X	X	X	X	X	1	0	1	1	Data Phase run cycle word read
DATA_RUN/READ	0	0	X	X	X	X	0	X	X	X	X	X	1	X	X	X	Data Phase run cycle read from D cache
SWAPPED_DATA_READ	0	0	X	X	0	X	X	X	X	X	X	X	1	X	X	X	Data Phase run cycle read from I cache
DATA_RUN/WR_BYTE	0	0	X	X	X	X	X	X	X	0	X	X	1	0	0	0	Data Phase run cycle single-byte write
DATA_RUN/WR_2-BYTE	0	0	X	X	X	X	X	X	X	0	X	X	1	0	0	1	Data Phase run cycle half word write
DATA_RUN/WR_3-BYTE	0	0	X	X	X	X	X	X	X	0	X	X	1	0	1	0	Data Phase run cycle tribyte write
DATA_RUN/WR_WORD	0	0	X	X	X	X	X	X	X	0	X	X	1	0	1	1	Data Phase run cycle word write
DATA_RUN/WRITE	0	0	X	X	X	X	X	X	X	0	X	X	1	X	X	X	Data Phase run cycle write
CP_TRANSFER	0	0	X	1	1	1	1	1	X	1	X	X	1	0	X	X	Coprocessor transfer

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Table 2-1 (Cont.)
Control Group Symbol Table (R3000_Ctrl)

Symbol	Run*	Phase	Exc*	XEn*	IRd*	IWr*	DRd*	DWr*	MemRd*	MemWr*	RdBusy	WrBusy*	Reset*	AccTyp2	AccTyp1	AccTyp0	Meaning
DATA_TRANSFER	0	0	X	X	X	X	X	X	X	X	X	X	1	0	X	X	Data Phase run cycle with data transfer scheduled
NO_DATA	0	0	X	X	X	X	X	X	X	X	X	X	1	1	X	X	Data Phase run cycle with no data transfer scheduled
DATA_RUN/ INTGR2M	0	0	0	X	X	X	X	X	X	X	X	X	1	X	X	X	Interrupt grant signal IntGr2M†
DATA_RUN	0	0	X	X	X	X	X	X	X	X	X	X	1	X	X	X	Data Phase run cycle
DATA_STALL_/ READ_RETRY	1	0	1	0	X	X	X	X	X	X	1	X	1	X	X	X	Read Retry caused by RdBusy
DATA_STALL/ RD_CACHED	1	0	1	0	X	X	X	0	X	X	X	X	1	X	X	X	Data Phase Stall cycle cached read
SWAPPED_ DATA_STALL/ RD_CACHED	1	0	1	0	X	0	X	X	X	X	X	X	1	X	X	X	Swapped Data Phase Stall cycle cached read
DATA_STALL/ RD_ UNCACHED	1	0	1	0	X	1	X	1	X	X	X	X	1	X	X	X	Data Phase Stall cycle uncached read
DATA_STALL/ RD_BYTE	1	0	1	0	X	X	X	X	X	X	X	X	1	X	0	0	Data Phase Stall cycle single-byte read
DATA_STALL/ RD_2-BYTE	1	0	1	0	X	X	X	X	X	X	X	X	1	X	0	1	Data Phase Stall cycle half word read
DATA_STALL/ RD_3-BYTE	1	0	1	0	X	X	X	X	X	X	X	X	1	X	1	0	Data Phase Stall cycle tribyte read
DATA_STALL/ RD_WORD	1	0	1	0	X	X	X	X	X	X	X	X	1	X	1	1	Data Phase Stall cycle word read
DATA_STALL/ READ	1	0	1	0	X	X	X	X	X	X	X	X	1	X	X	X	Data Phase Stall cycle read
DATA_STALL/ WR_BYTE	1	0	1	1	X	X	X	X	X	0	X	X	1	X	0	0	Data Phase Stall cycle single-byte write
DATA_STALL/ WR_2-BYTE	1	0	1	1	X	X	X	X	X	0	X	X	1	X	0	1	Data Phase Stall cycle half word write
DATA_STALL/ WR_3-BYTE	1	0	1	1	X	X	X	X	X	0	X	X	1	X	1	0	Data Phase Stall cycle tribyte write
DATA_STALL/ WR_WORD	1	0	1	1	X	X	X	X	X	0	X	X	1	X	1	1	Data Phase Stall cycle word write
DATA_STALL/ WRITE	1	0	1	1	X	X	X	X	X	0	X	X	1	X	X	X	Data Phase Stall cycle write
CP_STALL	1	0	0	X	X	X	X	X	X	X	X	X	1	X	X	X	Coprocessor Stall cycle
MP_STALL_ READ	1	0	1	1	X	X	0	X	X	1	X	X	1	X	X	X	Multiprocessor Stall cycle read
MP_STALL_ INVALIDATE	1	0	1	1	X	X	X	0	X	1	X	X	1	X	X	X	Multiprocessor Stall cycle write
DATA_STALL	1	0	X	X	X	X	X	X	X	X	X	X	1	X	X	X	Data Phase Stall cycle

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Table 2-1 (Cont.)
Control Group Symbol Table (R3000_Ctrl)

Symbol	Run*	Phase	Exc*	XEn*	IRd*	IWr*	DRd*	DWr*	MemRd*	MemWr*	RdBusy	WrBusy*	Reset*	AccTyp2	AccTyp1	AccTyp0	Meaning
MAIN_MEM_ DATA READ	X	0	X	0	X	X	X	X	X	X	X	X	1	X	X	X	Main memory Data Phase read
WRITE_ I CACHE_ ONLY	X	0	X	X	X	0	X	X	X	1	X	X	1	X	X	X	Instruction cache write
WRITE_ DCACHE_ ONLY	X	0	X	X	X	X	X	0	X	1	X	X	1	X	X	X	Data cache write
MAIN_MEM_ READ	X	X	X	0	X	X	X	X	X	X	X	X	1	X	X	X	Main memory read
MAIN_MEM_ WRITE	X	0	X	X	X	X	X	X	X	0	X	1	1	X	X	X	Main memory write
RESET_INST_ PHASE	X	1	X	X	X	X	X	X	X	X	X	X	0	X	X	X	Instruction Phase reset
RESET_DATA_ PHASE	X	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	Data Phase reset
RESET	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	Any reset

† Exc1W* and IntGr2M* are Run cycles with Exception* (Exc*) asserted as defined by the *MIPS R3000 Processor Interface*.
‡ These symbols may not display or trigger correctly at higher CPU clock rates due to the effects of the T_{SExc} timing delay
  specification. Refer to *Supplemental Timing Information* for additional information on the timing specifications.

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Section 3: INSTALLATION AND CONNECTIONS

This section contains detailed descriptions of how to do the following:

* install the disassembler software

* view the demonstration reference memory

* set up the disassembler software

* connect the DAS 9200 to the system under test (SUT)

* configure the probe adapter

You must install the microprocessor support software prior to invoking and setting up the disassembler. It does not matter if you install the software before or after making the DAS 9200 connections and configuring the probe adapter.

You should configure the probe adapter before connecting the DAS 9200 to the R3000 system. Configuring the probe adapter consists of setting two jumpers and (if necessary) selecting the correct replaceable socket for the probe adapter. Details on configuring the probe adapter are give later in this section.

The probe adapter is shipped with a 145-pin replaceable protective socket installed in addition to a 175-pin socket. If your R3000 system uses the R3000A microprocessor, you need to replace the 145-pin socket with the 175-pin socket. Refer to *Removing and Replacing Sockets* in Appendix C for instructions on replacing the protective sockets.

INSTALLING SOFTWARE

The R3000 support software sets up the DAS 9200 to acquire, disassemble, and display data from an R3000 system. To install the support software, the support application files on the 5 1/4-inch floppy disk must be copied to the DAS 9200 hard disk.

To install the software, follow these steps:

1. Power on the DAS 9200 and press the Select Menu key.

2. Select the Disk Services menu in the Utilities column.

3. Press F6: MOVE TO UTILITY.

4. Select Install Applications in the Operation field.

5. Press F8: EXECUTE OPERATION and follow the on-screen prompts.

If there is inadequate disk free space available on the hard disk, you must use the Remove Application or Delete File function of the Disk Services menu to free up enough disk space to install the software. The approximate space required to install the software is listed on the label of the floppy disk.

You cannot execute the disassembler from the floppy disk.

After the DAS 9200 successfully copies the application files from the floppy disk to the hard disk, the message **Application installation complete with no errors** appears on your screen. Remove the floppy disk and store it in a safe place in case you need to reinstall the software.

If you would like to see an example of R3000 bus activity with mnemonic disassembly, read the next discussion and procedure.

Viewing the Refmem Files

A reference memory file (called R3000_Demo) is provided for you to familiarize yourself with the way the disassembler displays R3000 instruction mnemonics. A second reference memory (called R3K_Timg_96) is provide for you to view the R3000 timing bus forms as discussed in Section 5. You can select either reference memory file to see how R3000 data is displayed without making any DAS 9200 connections to your system under test.

Both reference memory files are automatically installed when the disassembler software is installed on the hard disk. All the figures in Section 4 showing acquired data are from the R3000_Demo file. The data you acquire from your R3000 system will be different.

To view the reference memory files, use the following procedure:

1. Press the Select Menu key to return to the Menu Selection overlay.

2. Move the cursor to the Refmem column and select the reference memory you want to view.

3. Move the cursor to the Display column and select Disasm if you want to view the R3000_Demo file, or select timing if you want to view the R3K_Timg_96 timing refmem file.

4. Press F5: MOVE TO DISPLAY or the Return key to view the reference memory that you selected.

You can change the format of disassembled data from the Disassembly Format Definition overlay, which you access through the Disassembly menu. Hardware disassembly is the default format in the Disassembly menu. Examples of the disassembly formats are found under *Displaying Disassembled Data* in Section 4.

If there is not enough free space left on the hard disk, you can delete the R3000_Demo refmem file, the R3000_Addr symbol table, or the R3K_Timg_96 timing refmem file from the hard disk. These files are presented strictly for viewing and are not necessary to the operation of the disassembler.

Setting Up Disassembler Software

The microprocessor support package supplies the disassembler software and setup files for the data acquisition module to use to acquire and display instruction mnemonics. Setup files are supplied for the Channel, Clock, and Trigger menus. A Symbol file for the Control group is supplied for displaying data and to use in the Trigger menu. In addition, a Trigger library file , (called R3000_Lib) is provided to help you trigger on selected disassembled data. A format file is also provided for the Timing menu when performing hardware analysis (described in Section 5).

Before selecting and setting up the disassembler, read the descriptions of *R3000 System Requirements and Restrictions* in Section 1.

The 92DM74 software is designed to work with a single 92A96 Module. If your DAS 9200 configuration contains more than one 92A96 card in adjacent slots, you must reconfigure your 92A96 Module to operate as a single-card module. If you do not have the correct 92A96 Module configuration, the DAS 9200 will display the following message when you attempt to select the R3000 Support in the Configuration menu: **ERROR: Incompatible channel width detected. Restored the previous setup.** Refer to the *DAS 9200 System User's Manual* for information on using the System Configuration menu to configure your 92A96 Module.

You can invoke the disassembler and its associated setup files from the module's Configuration menu. Move the cursor to the Software Support field and select R3000 Support. The microprocessor support software automatically sets up the various module menus as soon as you select R3000 Support.

A detailed description of the disassembler setup follows. You can select the Channel, Symbol Editor, Clock, and Trigger menus to view default setups and files.

If you have more than one data acquisition module in the DAS 9200, you should apply slot number labels to various parts of the DAS 9200 equipment before setting up the disassembler. Refer to the *Labels* discussion in this section for a description of where to apply the slot number labels. These slot numbers will help you identify which data acquisition module is connected to the probe adapter in a multimodule system.

Channel Groups and Assignments

The disassembler relies on the presence of the signals and channel groups defined by the support software for the Address, Data, Jumper, and Control channel groups. The channel assignment table is located in Appendix C.

What You Can Change During Setup

You can change part of the module setup without affecting disassembly. You can change the trigger program in the Trigger menu and the display radix for any channel group in the Channel menu or Disassembly Format definition overlay.

You cannot change the channel grouping or name for the Address, Data, Jumper, or Control groups, the threshold voltage, or polarity and expect the disassembler to function properly.

However, you can change the R3000 signal connections, the channel grouping, and group name for the channels not required for mnemonic disassembly. Refer to the discussions on signals in Appendix B for a list of these signal connections. Refer also to the discussion on *Alternate Connections* in this section for a description of how to make connections to other signals in your R3000 system.

Symbol Tables

You can use symbol tables to display channel group information symbolically in the State and Disassembly menus and to control triggering. There is a symbol table file (named R3000_Ctrl) supplied by the disassembler software that replaces specific Control channel group values. Refer to *Triggering* and *Displaying the Address Group Symbolically* in Section 4 for more information on displaying symbolic values.

A second symbol table (called R3000_Addr) is provided with the 92DM74 software for use with the R3000_Demo reference memory file to demonstrate the use of a symbol table with the address group. You can delete this symbol table if you need more disk space on the DAS 9200; it is provided for demonstration purposes only.

Table 3-1 shows the name, bit pattern, and meaning for the symbols in the file R3000_Ctrl, the Control group symbol table.

Table 3-1
Control Group Symbol Table (R3000_Ctrl)

Symbol	Run*	Phase	Exc*	XEn*	IRd*	IWr*	DRd*	DWr*	MemRd*	MemWr*	RdBusy	WrBusy*	Reset*	AccTyp2	AccTyp1	AccTyp0	Meaning
INSTR_ STREAMING	0	1	X	0	X	X	X	X	X	X	X	X	1	X	X	X	Instruction fetched during streaming
SWAPPED_ INST_RUN	0	1	X	X	X	X	0	X	X	X	X	X	1	X	X	X	Swapped Instruction run cycle
INST_RUN/ EXC1W	0	1	0	X	X	X	X	X	X	X	X	X	1	X	X	X	Exception indication Exc1W†
INST_RUN	0	1	X	X	X	X	X	X	X	X	X	X	1	X	X	X	Instruction Phase of a run cycle
INST_STALL/ RETRY	1	1	X	0	X	X	X	X	X	X	1	X	1	X	X	X	Instruction Phase of a Stall, read with Retry
INST_FIXUP/ READ	1	1	0	0	X	X	X	X	X	X	X	X	1	X	X	X	Instruction Read from main memory during a Fixup cycle
INST_REFILL	1	1	1	0	X	X	X	X	X	X	X	X	1	X	X	X	Instruction Phase of a Refill cycle
INST_FIXUP	1	1	0	X	X	X	X	X	X	X	X	X	1	X	X	X	Instruction Phase of a Fixup cycle‡
INST_STALL	1	1	1	X	X	X	X	X	X	X	X	X	1	X	X	X	Instruction Phase of a Stall cycle‡
UNCACHED_ INST	X	1	X	0	X	1	X	1	X	X	X	X	1	X	X	X	Any uncached Instruction fetch
MAIN_MEM_ INST_READ	X	1	X	0	X	X	X	X	X	X	X	X	1	X	X	X	Read instruction from main memory
DATA_RUN/ RD_BYTE	0	0	X	X	X	X	0	X	X	X	X	X	1	0	0	0	Data Phase run cycle single-byte read
DATA_RUN/ RD_2-BYTE	0	0	X	X	X	X	0	X	X	X	X	X	1	0	0	1	Data Phase run cycle half word read
DATA_RUN/ RD_3-BYTE	0	0	X	X	X	X	0	X	X	X	X	X	1	0	1	0	Data Phase run cycle tribyte read
DATA_RUN/ RD_WORD	0	0	X	X	X	X	0	X	X	X	X	X	1	0	1	1	Data Phase run cycle word read
DATA_RUN/ READ	0	0	X	X	X	X	0	X	X	X	X	X	1	X	X	X	Data Phase run cycle read from D cache
SWAPPED_ DATA_READ	0	0	X	X	0	X	X	X	X	X	X	X	1	X	X	X	Data Phase run cycle read from I cache

(Cont.)

Table 3-1 (Cont.)
Control Group Symbol Table (R3000_Ctrl)

Symbol	Run*	Phase	Exc*	XEn*	IRd*	!Wr*	DRd*	DWr*	MemRd*	MemWr*	RdBusy	WrBusy*	Reset*	AccTyp2	AccTyp1	AccTyp0	Meaning
DATA_RUN/ WR_BYTE	0	0	X	X	X	X	X	X	X	0	X	X	1	0	0	0	Data Phase run cycle single-byte write
DATA_RUN/ WR_2-BYTE	0	0	X	X	X	X	X	X	X	0	X	X	1	0	0	1	Data Phase run cycle half word write
DATA_RUN/ WR_3-BYTE	0	0	X	X	X	X	X	X	X	0	X	X	1	0	1	0	Data Phase run cycle tribyte write
DATA_RUN/ WR_WORD	0	0	X	X	X	X	X	X	X	0	X	X	1	0	1	1	Data Phase run cycle word write
DATA_RUN/ WRITE	0	0	X	X	X	X	X	X	X	0	X	X	1	X	X	X	Data Phase run cycle write
CP_TRANSFER	0	0	X	1	1	1	1	1	X	1	X	X	1	0	X	X	Coprocessor transfer
DATA_ TRANSFER	0	0	X	X	X	X	X	X	X	X	X	X	1	0	X	X	Data Phase run cycle with data transfer scheduled
NO_DATA	0	0	X	X	X	X	X	X	X	X	X	X	1	1	X	X	Data Phase run cycle with no data transfer scheduled
DATA_RUN/ INTGR2M	0	0	0	X	X	X	X	X	X	X	X	X	1	X	X	X	Interrupt grant signal IntGr2M†
DATA_RUN	0	0	X	X	X	X	X	X	X	X	X	X	1	X	X	X	Data Phase run cycle
DATA_STALL_/ READ_RETRY	1	0	1	0	X	X	X	X	X	X	1	X	1	X	X	X	Read Retry caused by RdBusy
DATA_STALL/ RD_CACHED	1	0	1	0	X	X	X	0	X	X	X	X	1	X	X	X	Data Phase Stall cycle cached read
SWAPPED_ DATA_STALL/ RD_CACHED	1	0	1	0	X	0	X	X	X	X	X	X	1	X	X	X	Swapped Data Phase Stall cycle cached read
DATA_STALL/ RD_ UNCACHED	1	0	1	0	X	1	X	1	X	X	X	X	1	X	X	X	Data Phase Stall cycle uncached read
DATA_STALL/ RD_BYTE	1	0	1	0	X	X	X	X	X	X	X	X	1	X	0	0	Data Phase Stall cycle single-byte read
DATA_STALL/ RD_2-BYTE	1	0	1	0	X	X	X	X	X	X	X	X	1	X	0	1	Data Phase Stall cycle half word read
DATA_STALL/ RD_3-BYTE	1	0	1	0	X	X	X	X	X	X	X	X	1	X	1	0	Data Phase Stall cycle tribyte read
DATA_STALL/ RD_WORD	1	0	1	0	X	X	X	X	X	X	X	X	1	X	1	1	Data Phase Stall cycle word read
DATA_STALL/ READ	1	0	1	0	X	X	X	X	X	X	X	X	1	X	X	X	Data Phase Stall cycle read
DATA_STALL/ WR_BYTE	1	0	1	1	X	X	X	X	X	0	X	X	1	X	0	0	Data Phase Stall cycle single-byte write
DATA_STALL/ WR_2-BYTE	1	0	1	1	X	X	X	X	X	0	X	X	1	X	0	1	Data Phase Stall cycle half word write
DATA_STALL/ WR_3-BYTE	1	0	1	1	X	X	X	X	X	0	X	X	1	X	1	0	Data Phase Stall cycle tribyte write
DATA_STALL/ WR_WORD	1	0	1	1	X	X	X	X	X	0	X	X	1	X	1	1	Data Phase Stall cycle word write

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Table 3-1 (Cont.)
Control Group Symbol Table (R3000_Ctrl)

Symbol	Run*	Phase	Exc*	XEn*	IRd*	IWr*	DRd*	DWr*	MemRd*	MemWr*	RdBusy	WrBusy*	Reset*	AccTyp2	AccTyp1	AccTyp0	Meaning
																	Control Group Value
DATA_STALL/ WRITE	1	0	1	1	X	X	X	X	X	0	X	X	1	X	X	X	Data Phase Stall cycle write
CP_STALL	1	0	0	X	X	X	X	X	X	X	X	X	1	X	X	X	Coprocessor Stall cycle
MP_STALL_ READ	1	0	1	1	X	X	0	X	X	1	X	X	1	X	X	X	Multiprocessor Stall cycle read
MP_STALL_ INVALIDATE	1	0	1	1	X	X	X	0	X	1	X	X	1	X	X	X	Multiprocessor Stall cycle write
DATA_STALL	1	0	X	X	X	X	X	X	X	X	X	X	1	X	X	X	Data Phase Stall cycle
MAIN_MEM_ DATA READ	X	0	X	0	X	X	X	X	X	X	X	X	1	X	X	X	Main memory Data Phase read
WRITE_ I CACHE_ ONLY	X	0	X	X	X	0	X	X	X	1	X	X	1	X	X	X	Instruction cache write
WRITE_ DCACHE_ ONLY	X	0	X	X	X	X	X	0	X	1	X	X	1	X	X	X	Data cache write
MAIN_MEM_ READ	X	X	X	0	X	X	X	X	X	X	X	X	1	X	X	X	Main memory read
MAIN_MEM_ WRITE	X	0	X	X	X	X	X	X	X	0	X	1	1	X	X	X	Main memory write
RESET_INST_ PHASE	X	1	X	X	X	X	X	X	X	X	X	X	0	X	X	X	Instruction Phase reset
RESET_DATA_ PHASE	X	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	Data Phase reset
RESET	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	Any reset

† Exc1W* and IntGr2M* are Run cycles with Exception* (Exc*) asserted as defined by the *MIPS R3000 Processor Interface.*

‡ These symbols may not display or trigger correctly at higher CPU clock rates due to the effects of the T_{SExc} timing delay specification. Refer to *Supplemental Timing Information* for additional information on the timing specifications.

Merging Symbol Tables

Only one symbol table can be used with each channel group. If you want to use more than one symbol table, you must merge them to make one symbol table. Note that symbol matching is performed by searching sequentially from the beginning of the symbol table. Therefore, the symbol ordering is important for both range and pattern types of symbol tables. Refer to the *DAS 9200 System User's Manual* for more information on symbol tables.

To merge symbol tables together, follow these steps:

1. Select the Symbol Editor menu from the Menu Selection overlay.

2. Press F2: FILE FUNCTIONS.

3. Select Open File in the Function field.

4. Select New File in the Edit Status field.

5. Enter a new symbol table file name.

6. Select Range or Pattern in the Table Type field depending on whether your symbol table file is a Range file or Pattern file.

7. Press F5: EXECUTE FUNCTION.

8. Select Merge Files in the Function field.

9. Determine the first file to start the new symbol table in the File Name to Merge field.

10. Press F5: EXECUTE FUNCTION.

11. Press F8: EXIT & SAVE.

12. If your symbol table file is a Range file, enter the base address of where your symbols are located in your system's memory in the Base Address field. Then select Relative to Base in the Mode field.

13. Move the cursor to the appropriate location in the table if the next file to be merged is to be placed at the end of the current symbol table.

14. Press F2: FILE FUNCTIONS.

15. Select the next file to merge with the new table in the File Name to Merge field.

16. Press F5: EXECUTE FUNCTION.

17. Press F8: EXIT & SAVE.

18. Repeat steps 13 through 17 to merge additional tables to the new table.

19. Select the Channel menu.

20. Change the file name of the symbol table for the Control group (or whichever group's symbol table you are replacing) to the one that you specified in step 5.

You do not have to re-create a new table each time you move the tables in your system as long as the relative difference in address locations doesn't change. If you move the tables in your system without changing the relative difference in address locations, you only need to redefine the base address for the symbol table.

Copying and Editing the Predefined Symbol Tables

You cannot directly edit the R3000_Ctrl or the R3000_Addr symbol tables, but you can make a copy of them and then edit the copies for your specific use.

To create a new symbol table, follow these steps:

1. Select the Symbol Editor menu.

2. Press F2: FILE FUNCTIONS.

3. Select Open File in the Function field.

4. Select New File in the Edit Status field.

5. Enter a new symbol table file name.

6. Select Pattern or Range in the Table Type field to match the symbol table you are copying.

7. Press F5: EXECUTE FUNCTION.

8. Select Merge Files in the Function field.

9. Select the file to base your new symbol table on, such as the R3000_Ctrl file.

10. Press F5: EXECUTE FUNCTION.

11. Press F8: EXIT & SAVE.

12. Edit the file as desired. Refer to your *DAS 9200 System User's Manual* for information on editing the symbol table.

13. Select the Channel menu.

14. Change the file name of the symbol table for the Control group (or whichever group's symbol table you are replacing) to the one that you specified in step 5.

LABELS

The probe connectors, cables, and interface housings for the 92A96 Module have color-coded labels. Table 3-2 shows the color of both the probe connector and interface housing labels, as well as the module section and clock assignments.

Table 3-2
Label Information

Label Color	Sections	Clock
Orange	A0, A1, C0	Ck 0
Green	A2, A3, C1	Ck 1
Blue	D0, D1, C2	Ck 2
Gray	D2, D3, C3	Ck 3

Each interface housing connects to three 8-channel probes and a single clock probe. Individual 8-channel probes are labeled with ground and color-coded channel assignments (7-0) only as shown in Figure 3-1.
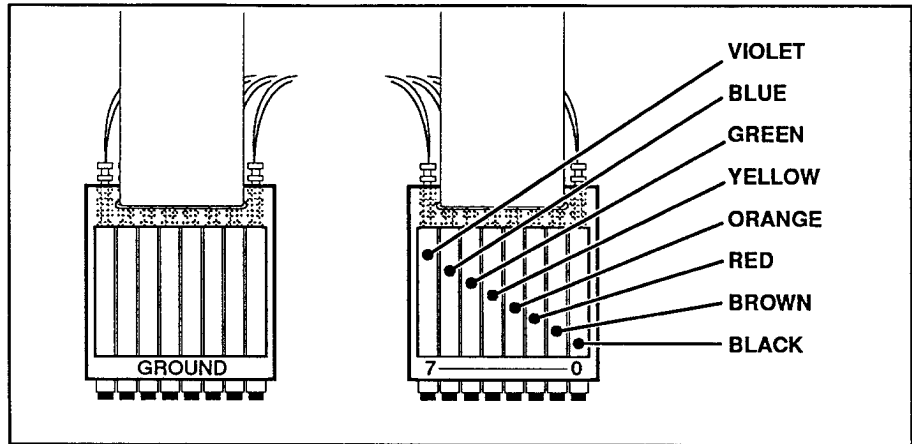
Figure 3-1.   Probe channel color and labels on an 8-channel probe.

You should apply slot number labels as shown in Figure 3-2 if there is more than one 92A96 Module in the DAS 9200. These slot numbers will help you identify which module is connected to the probe adapter in a multimodule system.
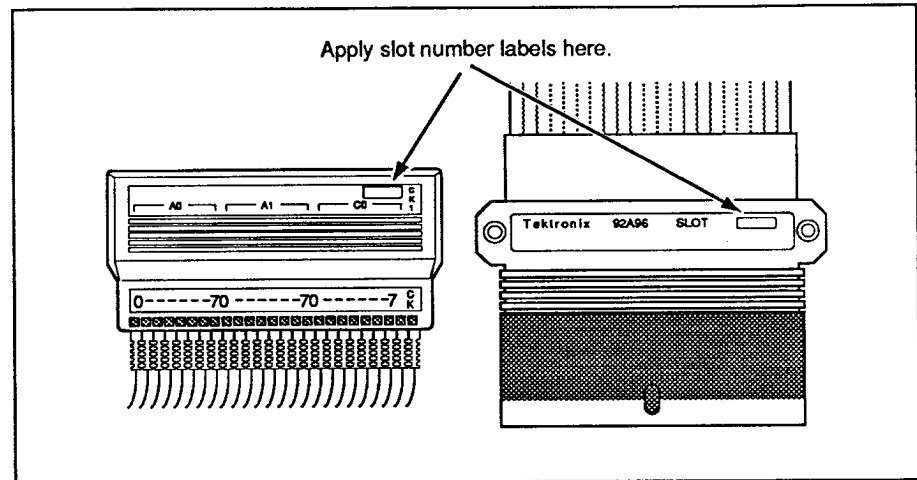
Figure 3-2. Applying slot number labels.

CONFIGURING THE PROBE ADAPTER

The R3000 probe adapter has two user-configurable jumpers that must be configured before you acquire data the first time.

The Big/Little Endian jumper lets you select the byte ordering. Determine which byte ordering is required by your system and set the jumper accordingly. The jumper is shipped in the Big-Endian position. The concept of Big-Endian and Little-Endian as it applies to the R3000 is explained in your R3000 vendor's documentation.

The Timing/Normal jumper lets you configure the disassembler to run in Timing (Transparent) mode. The Timing mode bypasses the additional latching or stretching of selected signals on the probe adapter. Signals that are buffered or latched in the Normal mode are buffered in the Timing mode. For Disassembly purposes, you should leave the jumper in the Normal position. Determine whether or not you need to run in Transparent mode and set the jumper as described in Section 5.

CONNECTING THE PROBE ADAPTER

Before acquiring data, you must connect the probe adapter to the clock and 8-channel probes for the 92A96 Module being used and to the SUT. Your R3000 system must have a minimum amount of clear space surrounding the microprocessor to accommodate either the standard or optional probe adapter. Figures C-1 and C-2 in *Appendix C: Service Information* show these dimensions.

This discussion describes how to connect the following:

- the probes to the probe adapter
- the probe adapter to the SUT

> **CAUTION**

> *Static discharge can damage the microprocessor, 8-channel probes, clock probes, or the 92A96 Module. To prevent static damage, observe the following precautions while following all connection procedures.*

> *Handle the microprocessor only in a static-free environment.*

> *Always wear a grounding wrist strap, or similar device, while handling the microprocessor and probe adapter.*

> *Discharge stored static electricity from the probe adapter by touching any of the ground pins (the row of pins closest to the edge of the probe adapter circuit board).*

The 92A96 probe cables should already be connected to the probe connectors. If not, refer to your module user's manual for the connection procedures.

Connecting the Probes to the Probe Adapter

To connect the 92A96 Module clocks and 8-channel probes to the probe adapter, refer to Figure 3-3 and use the following procedure. If your podlets are not installed in a podlet holder, or are not installed in the proper order, refer to *Removing and Replacing Podlets* in Appendix C.

1. Use the antistatic shipping material to support the probe adapter while connecting the clock and 8-channel probes as shown in Figure 3-3. This prevents the circuit board from being flexed and the socket pins from being bent.

Hold the 8-Channel probes by the podlet holder when connecting them to the probe adapter. Do not hold them by the cables or neck of the podlets.
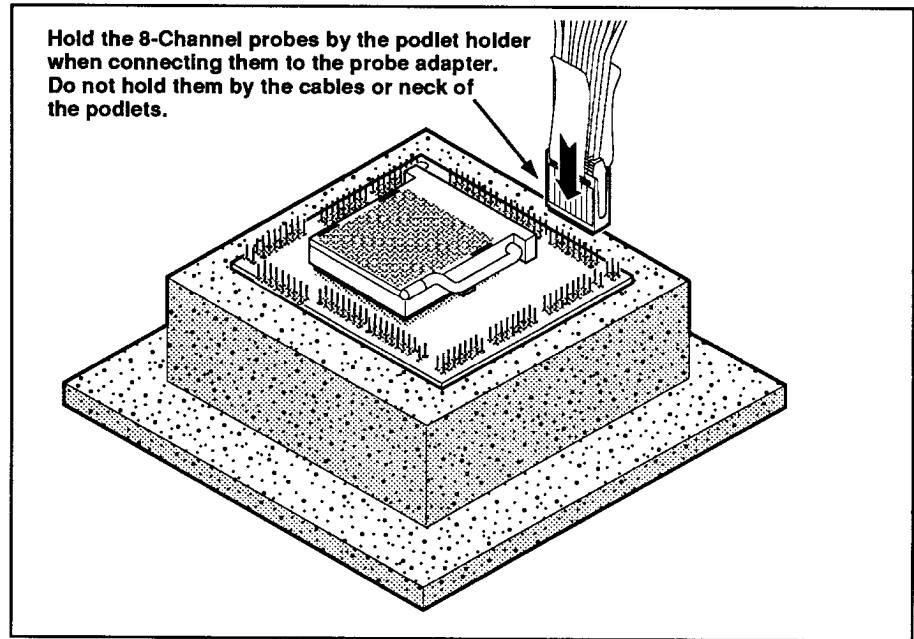
Figure 3-3.   Connecting the probes to the probe adapter.

> ┌─────────────────┐
> │   *CAUTION*   │
> └─────────────────┘

Connect only the signal connectors to the signal pins and the ground connectors to the ground pins. Connecting any R3000 signal to a probe adapter ground pin can damage the microprocessor or the probe adapter circuitry.

2. Refer to Figure 3-4 and line up each 8-channel probe with the corresponding section name printed on the probe adapter circuit board. The interface housing label indicates the group to which each 8-channel probe connects. All square pins closest to the edge of the circuit board connect to ground.
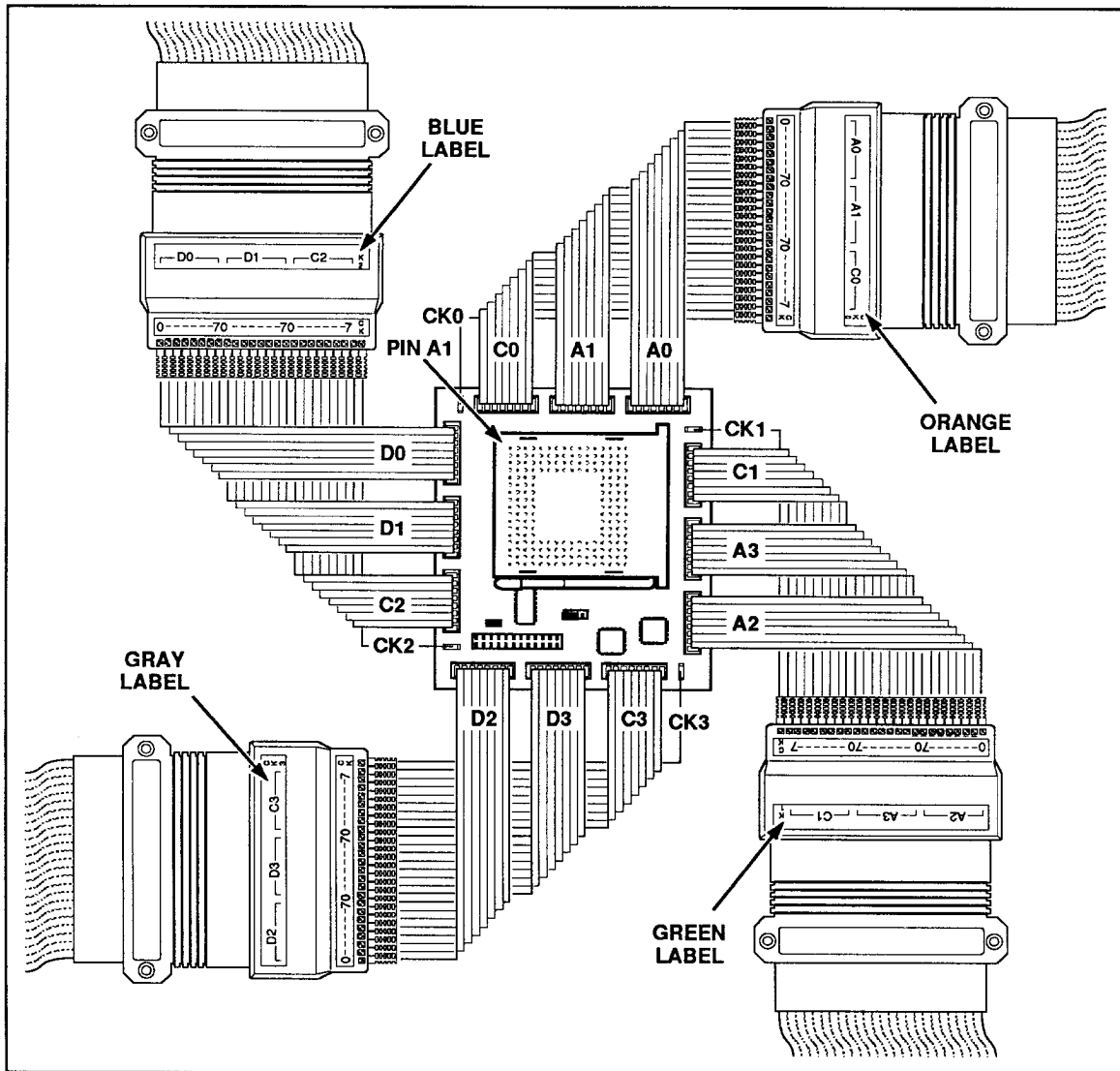
Figure 3-4. Connections from the 92A96 probe cables to the probe adapter.

3. Push each 8-channel probe over the assigned group of square pins. Channel numbers printed on the circuit board must match the channel numbers on the 8-channel probes.

4. Line up the label on each clock probe with the corresponding pair of square pins on the probe adapter. Be sure to orient the clock probe ground and signal connector to the clock ground and signal square pins on the probe adapter.

5. Push each clock probe over the assigned square pins.

Placing the Probe Adapter in the SUT

After you verify that you have the correct replaceable PGA socket (145-pin for R3000 systems and 175-pin for R3000A systems) installed on the probe adapter and after you connect all the clock and 8-channel probes to the probe adapter, you can place the probe adapter in the R3000 system. To place the probe adapter in the SUT, refer to Figure 3-5 and follow this procedure:

1. Turn off the power to the SUT. (It is not necessary to power down the DAS 9200.)

NOTE

If your SUT has a ZIF socket with a lever attached, you might need to remove the protective socket from the bottom of the probe adapter, place it in your system's ZIF socket, close the ZIF socket, and install the probe adapter in the protective socket. Refer to Removing and Replacing Sockets *in Appendix C for information on removing the protective sockets from the probe adapter.*

2. Carefully remove the microprocessor from your system.

3. Carefully plug the probe adapter into the R3000 socket of the SUT. Be sure to align pin A1 of the probe adapter to pin A1 of the system socket.

4. Open the ZIF socket on the probe adapter by pulling the lever up and away from the socket.

```
┌─────────────────┐
│    CAUTION      │
└─────────────────┘
```

*The microprocessor can be permanently
damaged if you insert it improperly on the probe
adapter. Pin A1 on the microprocessor must
align with pin A1 on the ZIF socket of the probe
adapter.*

*Offsetting the probe adapter by one row of pins on
the SUT can damage the microprocessor, probe
adapter, or SUT. The probe adapter must align
with pin A1 of the SUT. See Figure 2-3 for proper
alignment of pin A1 on the microprocessor, the ZIF
socket, and the R3000 system socket.*
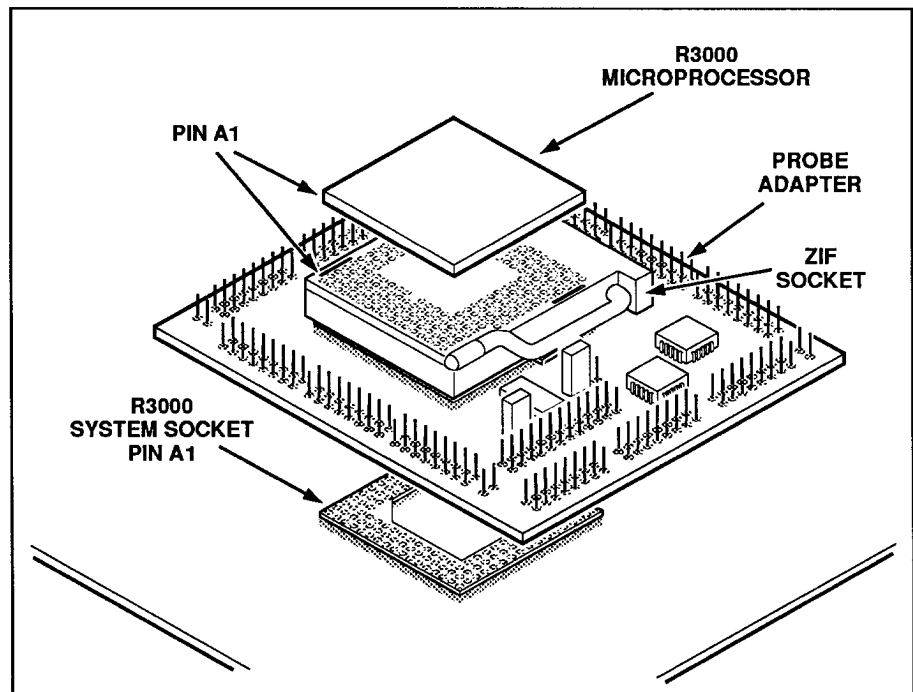
Figure 3-5. Placing the probe adapter in the R3000 system. The clock
and 8-channel probes should already be connected before placing
the probe adapter in the system. They are not shown connected
in this figure because they would obscure the detail.

5. Carefully plug the microprocessor into the ZIF socket so
   that pin A1 of the microprocessor is inserted into pin A1 of
   the ZIF socket. Push the ZIF socket's lever down to lock the
   ZIF socket in the closed position.

Connecting the Interface Housings

The probe cables and interface housings may already be connected. If they are not connected, refer to Figure 3-6 and follow this procedure:

1. Select an interface housing with a label color that matches a label color on one of the 92A96 probe cables.

2. Line up the key on the loose connector end of the probe cable with the key slot on the interface housing and connect them.

3. Repeat steps 1 and 2 for each of the three remaining probe cables.
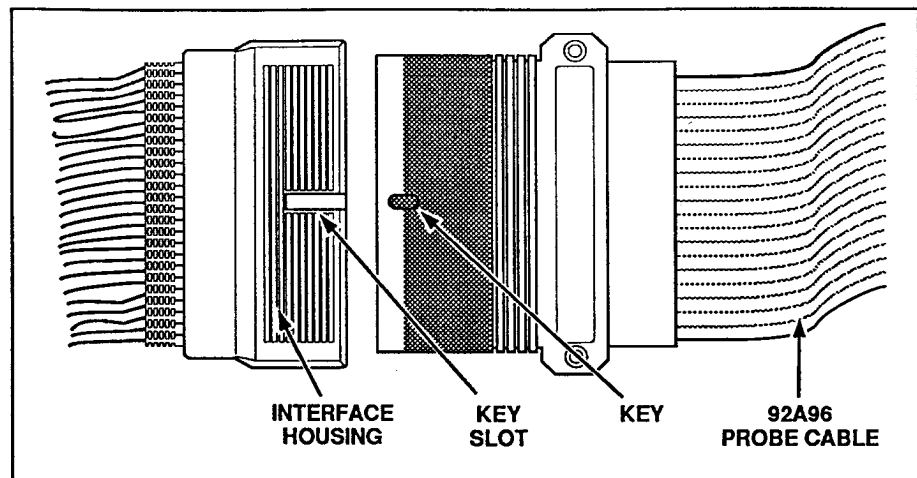
Figure 3-6. **Connecting the interface housing to the 92A96 probe cable.** The interface housing label is on the other side of the housing and not visible in the figure.

Alternate Connections

There are 15 channels that connect to the R3000 system but are not used for mnemonic disassembly. Some of these signals may be meaningful during disassembly and others are only useful for hardware analysis. These signals and their uses are described under *Acquired Signals Not Required for Disassembly* in Appendix B.

You can use any of these channels for general purpose use to acquire data from other parts of your system. Table 3-3 shows the sections and channels you can connect to other signals in your system.

Table 3-3
Channels Available for Alternate Connections

Section/ Channel	Signal Name
C0:7	DRW_Fixup*=†
C0:6	TagV
C0:5	Int*(5)
C0:4	Int*(4)
C0:3	Int*(3)
C0:2	Int*(2)
C0:1	Int*(1)
C0:0	Int*(0)
C1:7	CpSync*
C1:5	CpCond3 (AdrLo17)
C1:4	CpCond2 (AdrLo16)
C1:3	CpCond1
C1:2	CpCond0
C1:1	BusError*
C1:0	CpBusy

† DRW_Fixup*= is a synthesized signal that is the negative logical OR of the DRd*, DWr*, and Fixup* signals

You can separate the individual channels (podlets) from the 8-channel probes and connect them to other signals in your R3000 system. Refer to *Removing and Replacing Podlets* in Appendix C of this manual for information on how to separate podlets from an 8-channel probe. Also refer to your data acquisition user's manual for information on general purpose applications of the 92A96 Module.

NOTE

*Be sure to connect all podlet ground channels to
the ground in the R3000 system when making
any alternate connections.*

You may also need to use a flying leadset (Tektronix part
number 196-3347-00) and attach grabber tips (Tektronix part
number 020-1386-01) to make alternate connections.

If you want to use these channels for other purposes, you
probably will want to change the channel grouping in the
Channel menu. To change the default channel grouping, follow
these steps:

1. While in the Channel menu, press F8: ADD. Select Add a
   Group and press the Return key.

2. The cursor will appear in the Group Name field. You can
   enter a new group name or use the default group name.

3. Move the cursor to the Section field and enter a section
   name. Table 3-3 shows the sections and channels you can
   use to define new groups without disturbing disassembly.

4. Add channels to the new group by entering channel
   numbers in the Channel field. The DAS 9200 automatically
   removes channels from existing channel groups as they are
   used to create new channel groups. However, this means
   that any symbol tables that you created for the modified
   groups may no longer be correct.

5. After the new groups are defined, press the Select Menu
   key to exit the Channel menu.

Section 4: ACQUIRING AND VIEWING DISASSEMBLED DATA

The primary function of the disassembler is to assist you during the design period when you try to execute new or untested software on your prototype R3000 hardware. A second use is to test new software on an R3000 system that is already integrated. This section describes how to acquire data for viewing in the Disassembly menu.

After you install the microprocessor support software, make all the connections between the DAS 9200 and the SUT and select the R3000 Support, you are ready to complete the setup for the data acquisition module. To complete the setup, you need to choose a clock type (or use the default) and define a trigger program (or use the default).

CLOCKING

You can use the Clock menu to set clocking choices to control data sampling. The 92DM74 software offers a customized clocking selection for the R3000 microprocessor. This clocking choice (Custom) is the default selection whenever you select the R3000 Support in the Configuration menu.

The 92DM74 software provides six modes for acquiring R3000 data. You can select the clocking modes by selecting the appropriate fields in the Clock menu.

Included Stall Phases. This field lets you decide how you want the disassembler to handle Stall Phases. The following three selections are available: Fixup and First Refill (default selection), Fixup and All Refills, and All.

Run Cycle Data Phases. This field establishes how the disassembler will handle the Run Cycle Data Phases. The following two selections are available: Excludes Unused & CP Xfer and Includes All.

Refer to *Custom Clocking* in Appendix B for details about the individual clocking selections. Figure 4-1 shows the Clock menu with the two clocking fields.
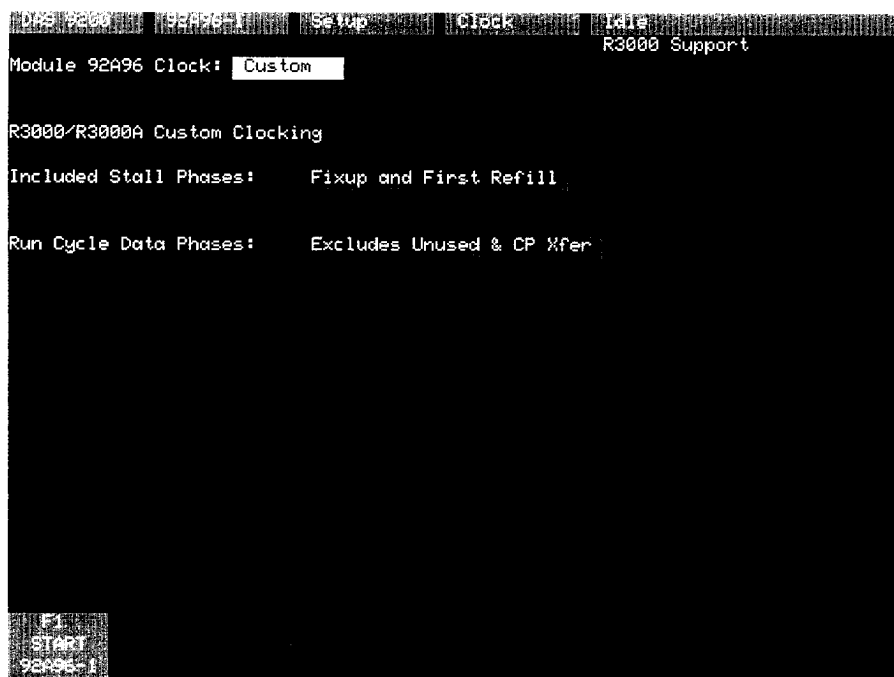
Figure 4-1. Clock menu.

Disassembly normally will not be correct with the Internal or External clocking modes. Refer to *Section 5: Hardware Analysis* for a description of using these other clock selections with this microprocessor support package.

TRIGGERING

All the Trigger menu selections currently available for your data acquisition module are still valid for disassembly. Refer to your module user's manual for a list and description of the selections.

A Trigger library called R3000_Lib is provided with two entries to help trigger on instruction fetches and data reads where the possibility of a cache miss can cause a simple address comparison routine to trigger on the wrong cycle. When you use either Trigger library entry, note that the trigger point can be delayed until the next run cycle to properly handle the possibility of a cache miss.

Because the R3000 microprocessor performs address translation on-chip, all addresses specified in the Trigger menu should be translated (physical) addresses. The address translation is always done for certain sections of the memory map.

When you specify an instruction address, it is sometimes necessary to specify the two least-significant address bits as "don't care bits". This is necessary because the R3000 does not always hold these address bits at zero when reading instructions from cache after data transfers.

The DAS 9200 makes it possible to cross-trigger with other modules or to an external instrument. You may want to consider sending or receiving a signal to or from another DAS 9200 module, or to the Trig In/Out SMB connector on the module. You should refer to your *DAS 9200 System User's Manual* for a description of defining and using signals and to specific module user's manual for a description of using the Trig In/Out SMB connector.

Refer to 92A96 Data Acquisition Module User's Manual for a details on using the Trigger Library.

ACQUIRING DATA

After you set up the disassembler to acquire data from your R3000 system, you can press F1: START to begin the acquisition. After satisfying the trigger program and filling acquisition memory, the DAS 9200 displays data in the menu and format last used. The default display menu is State. You change the display menus from the Menu Selection overlay (press the Select Menu key).

If the trigger is not located within a few moments, the DAS 9200 displays the Monitor menu showing the progress of the acquisition. You should check the trigger program when this occurs. Also refer to *Appendix A: Error Messages and Disassembly Problems* for a description of typical problems and possible solutions.

You can manually stop an acquisition by pressing F1: STOP. However, if you stop the acquisition while the Monitor menu is being displayed, the DAS 9200 will not automatically switch to the display menu; you need to manually switch to the display menus to view the acquired data.

DISPLAYING DISASSEMBLED DATA

The DAS 9200 displays disassembled data in the Disassembly menu. This menu shows the disassembled bus cycles, instruction mnemonics, operands and addresses, and data values.

You can display the disassembled data in different formats. You can select the display format and tailor it for your application using the Disassembly Format Definition overlay. Detailed information on this overlay is provided later in this section.

Display Formats

The R3000 disassembler software provides four formats for displaying disassembled data: Hardware, Software, Control Flow, and Subroutine. The Hardware format shows all acquired cycles and bus mnemonics in the order they occurred. The Software format suppresses all unnecessary stall cycles, cache misses, and all data transfers providing you with a display menu that looks similar to an assembly language program listing. The Control Flow format only displays the instructions that change the control flow of the microprocessor. The Subroutine format only displays subroutine calls, exceptions, and returns. You can further define how the data is displayed within the four formats by selecting display options with the Disassembly Format Definition overlay.

Figure 4-2 shows an example of the Disassembly menu.

```
Cursor:        1519                                          R3000 Support
Sequence   Address   Data       Mnemonics                             Timestamp
--------------------------------------------------------------------------------
     1247  1FC1617C  8F420008   LW        V0,0008(K0)                      690 ns
     1269  1FC16180  401A7000   MFC0      K0,EPC                           690 ns
     1291  1FC16184  00000000   NOP                                        690 ns
     1305  1FC16188  03400008   JR        K0                               430 ns
     1319  1FC1618C  42000010   RFE                                        440 ns
     1333  1FC14948  80434013   LB        V1,4013(V0)                      440 ns
     1347  1FC1494C  A0834010   SB        V1,4010(A0)                      440 ns
     1361  1FC14950  A0834011   SB        V1,4011(A0)                      440 ns
     1381  1FC14954  A0434012   SB        V1,4012(V0)                      620 ns
     1401  1FC14958  A0434013   SB        V1,4013(V0)                      630 ns
     1421  1FC1495C  A8434011   SWL       V1,4011(V0)                      620 ns
     1441  1FC14960  B8434014   SWR       V1,4014(V0)                      620 ns
     1461  1FC14964  34040001   ORI       A0,ZERO,0001                     630 ns
     1481  1FC14968  00800018   MULT      A0,ZERO                          620 ns
     1495  1FC1496C  00002812   MFLO      A1                               440 ns
     1519--1FC14970--00A00001A--DIV-------A1,ZERO-------------------------750-ns
     1533  1FC14974  34060003   ORI       A2,ZERO,0003                     440 ns
     1547  1FC14978  44861000   MTC1      A2,F2                            440 ns
     1561  1FC1497C  00000000   NOP                                        430 ns
     1575  1FC14980  46801080   CVT.S.W   F2,F2                            440 ns
     1589  1FC14984  00000000   NOP                                        440 ns
     1603  1FC14988  44061000   MFC1      A2,F2                            440 ns
     1617  1FC1498C  00000000   NOP                                        440 ns
              F2                    F4        F5
            SPLIT                 MARK      DEFINE
            DISPLAY               DATA      FORMAT
```

Figure 4-2. Disassembly menu.

No matter which display format you decide to use, the disassembler software displays information in the Disassembly menu in columns. The display order of the column is the set up by default; however, you can use selections in the Disassembly Format Definition overlay to turn other display groups on or add groups by assigning them a different group name. You can save the display setups in a format file and then restore them whenever you need them.

The following paragraphs briefly describe the columns displayed in the Disassembly menu:

* **Sequence Column.** The sequence column shows the sequence number of the data displayed on that line. The cursor field in the upper-left corner of the menu displays the sequence number of the current cursor location.

* **Address and Data Group Columns.** The address and data group columns show values for both the address and data bus at each sequence. You can display the Address group either symbolically or as an eight-digit hexadecimal value. The Data group is always displayed as an eight-digit hexadecimal value. When you select the Symbolic radix for a channel group, you must specify a symbol table for that group, then the group will be displayed symbolically. To display the Address group symbolically, refer to *Displaying the Address Group Symbolically* in this section.

  Gaps in the acquired data, caused by the data qualification specified in the Trigger menu, are indicated by a gray background behind the address and data groups. Dashed lines in a data sample represent invalid data bytes.

* **Instruction Mnemonics Group Column.** The instruction mnemonics column shows the disassembled R3000 cycles and instructions. The disassembler software displays disassembled instructions and operands as they are described in the *mips RISC Architecture* (Prentice Hall, 1988).

  The disassembler normally uses software names for the CPU general purpose registers. You can change a selection in the Disassembly Format Definition overlay to use hardware names. The disassembler uses F0–F31 for the R3010 Floating Point Coprocessor general registers and descriptive names for the coprocessor control registers.

The disassembler displays immediate data as hexadecimal values. Jump instructions and PC (program counter)-relative branches will have absolute addresses calculated and displayed in a symbolic or hexadecimal format matching the format selected for the address group. Be aware that the absolute address calculated for jump and branch instructions can sometimes be wrong if the memory management maps adjacent pages differently or if the instruction is next to qualification gaps or at the end of acquired data.

- **Timestamp Column.** The timestamp column shows the timestamp value, when you choose to display the timestamp values. You can use the Timestamp field of the Disassembly Format Definition overlay to select Absolute, Relative, or Off.

  Timestamp values show the amount of time that has elapsed between data samples. An Absolute timestamp shows the amount of time elapsed between the start of the acquisition and the current sample (the first sample can have a non-zero timestamp). A Relative timestamp shows the elapsed time between the previous and current sample. The Delta timestamp shows the elapsed time between the data sample that you mark with a delta (Δ) and each previous and subsequent sample. (To place the delta mark on a sample, use F4: MARK DATA from the Disassembly menu.)

  Cycles are assigned the value of the timestamp counter at the time that the 92A96 master clock occurs. Because the timestamp counter changes in 10 ns increments, timestamps for data acquired from an R3000 system with a clock rate that is not synchronous with the timestamp counter are slightly skewed. For example, data acquired from an R3000 system with a clock rate of 16 MHz (31 ns per half-clock sample) would be assigned a relative timestamp of either 30 or 40 ns. This skewing is not cumulative.

Hardware Display Format

In the Hardware format, all bus cycles are shown in the order that they occurred. Instruction mnemonics are displayed on the appropriate Instruction Phases. Non-instruction bus cycles are displayed as 32-bit wide data transactions. Invalid data bytes are represented as dashes.

Figure 4-3 shows the Hardware display format.

```
Refmem         R3000 Demo   Display      Disasm
Cursor:    1642                                       R3000 Support
Sequence  Address   Data      Mnemonics                            Timestamp
------------------------------------------------------------------------------
   1631  1FC14990  AC464020  SW      R6,4020(R2)              30 ns
   1632  9120C000  --------  ( DATA STALL )                   30 ns
   1633  00414994  0000000C  ( INST MISS )                    30 ns
   1634  0041C000  --------  ( NO DATA )                      40 ns
   1635  00414998  0000000C  ( INST STALL )                   30 ns
   1636  1FC14994  --------  ( DATA STALL )                   30 ns
   1637  1FC14994  0000000C  ( INST STALL )                   30 ns
   1638  1FC14994  --------  ( DATA STALL )                   30 ns
   1639  1FC14994  0000000C  ( INST STALL )                   30 ns
   1640  1FC14994  --------  ( DATA STALL )                   30 ns
   1641  1FC14994  0000000C  ( INST STALL )                   30 ns
   1642--1FC14994----------- (-DATA-STALL-)-----------------40-ns
   1643  1FC14994  0000000C  ( INST STALL )                   30 ns
   1644  1FC14994  --------  ( DATA STALL )                   30 ns
   1645  1FC14994  0000000C  SYSCALL                          30 ns
   1646  9120C000  --------  ( DATA STALL )                   30 ns
   1647  00414998  0000000C  ( NOT EXECUTED )                 30 ns
   1648  00014020  40400000  ( CACHED WRITE )                 30 ns
   1649  0041499C  0FF0586E  ( NOT EXECUTED )                 40 ns
   1650  0041C00C  --------  ( NO DATA )                      30 ns
   1651  00000080  3C1AA000  LUI     R26,A000                 30 ns
   1652  0000C00C  --------  ( NO DATA )                      30 ns
   1653  00000084  275A2418  ADDIU   R26,R26,2418             30 ns
             F2                F4       F5
           SPLIT             MARK     DEFINE
          DISPLAY            DATA     FORMAT
```

Figure 4-3. Hardware display format. The disassembler is set up to use hardware names (R0–31).

Software Display Format

In the Software format, only instructions are displayed. All other cycle types are suppressed. Figure 4-4 shows the Software display format.

```
Cursor:        1645                                          R3000 Support
Sequence  Address   Data      Mnemonics                               Timestamp
--------------------------------------------------------------------------------
    1481  1FC14968  00800018  MULT     A0,ZERO                          620 ns
    1495  1FC1496C  00002812  MFLO     A1                               440 ns
    1519  1FC14970  00A0001A  DIV      A1,ZERO                          750 ns
    1533  1FC14974  34060003  ORI      A2,ZERO,0003                     440 ns
    1547  1FC14978  44861000  MTC1     A2,F2                            440 ns
    1561  1FC1497C  00000000  NOP                                       430 ns
    1575  1FC14980  468010A0  CVT.S.W  F2,F2                            440 ns
    1589  1FC14984  00000000  NOP                                       440 ns
    1603  1FC14988  44061000  MFC1     A2,F2                            440 ns
    1617  1FC1498C  00000000  NOP                                       440 ns
    1631  1FC14990  AC464020  SW       A2,4020(V0)                      430 ns
    1645—1FC14994—0000000C—SYSCALL————————————————————————————————————440—ns
    1647  00414998  0000000C  ( NOT EXECUTED )                          60 ns
→M  1649  0041499C  0FF0586E  ( NOT EXECUTED )                          70 ns
    1651  00000080  3C1AA000  LUI      K0,A000                          60 ns
    1653  00000084  275A2418  ADDIU    K0,K0,2418                       60 ns
    1655  00000088  AF410004  SW       AT,0004(K0)                      60 ns
    1657  0000008C  AF5C0070  SW       GP,0070(K0)                      60 ns
    1659  00000090  AF420008  SW       V0,0008(K0)                      70 ns
    1661  00000094  24020001  ADDIU    V0,ZERO,0001                     60 ns
    1669  00000098  3C019FC1  LUI      AT,9FC1                         250 ns
    1677  0000009C  24216000  ADDIU    AT,AT,6000                      250 ns
    1679  000000A0  00200008  JR       AT                               60 ns
          F2                        F4        F5
          SPLIT                     MARK      DEFINE
          DISPLAY                   DATA      FORMAT
```

Figure 4-4. Software display format. The disassembler is set up to use software names.

Control Flow Display Format

The Control Flow display format only displays instructions that change the control flow. Instructions that do not actually change the control flow are not displayed, such as a conditional branch that is not taken. Figure 4-5 shows the Control Flow display format.

Instructions that unconditionally cause a change in the flow of control in an R3000 microprocessor are: J, JAL, JALR, JR, BREAK, SYSCALL, and reserved opcodes.

Instructions that can conditionally generate a change in the flow of control based on a value comparison or coprocessor condition signal are:

BCzF	BCzT	BEQ	BGEZ	BGTZ
BLEZ	BLTZ	BNE	BGEZAL	BLTZAL

In addition the RFE instruction and any instructions fetched from one of the five fixed exception entry hexadecimal locations (which appear at physical addresses 0000 0000, 0000 0080, 1FC0 0100, 1FC0 0180, or 1FC0 0000) are also displayed in the Control Flow display format to improve the visibility of exception processing.

Figure 4-5. Control Flow display format.

Subroutine Display Format

The Subroutine display format displays subroutine calls and returns only. The displayed subroutine calls and returns include exceptions and returns from exceptions. Subroutine calls that are not taken are not displayed. Figure 4-6 shows the Subroutine display format.

Instructions that unconditionally generate a subroutine call or return in an R3000 microprocessor include BREAK, SYSCALL, JAL, JALR, RFE, and JR R31.

Instructions that can conditionally appear in the Subroutine display format are BGEZAL and BLTZAL. Any instructions fetched from one of the five fixed exception entry hexadecimal locations (0000 0000, 0000 0080, 1FC0 00100, 1FC0 0180, or 1FC0 0000) are also displayed to improve the visibility of exception processing.

```
Cursor:        1651                                          R3000 Support
Sequence   Address    Data      Mnemonics                              Timestamp

    357    1FC1618C   42000010   RFE
    709    00000080   3C1AA000   LUI       K0,A000                      11.000 μs
   1319    1FC1618C   42000010   RFE                                    19.060 μs
   1645    1FC14994   0000000C   SYSCALL                                10.190 μs
   1651 ──00000080──3C1AA000──LUI────────K0,A000────────────────────────190─ns
   2267    1FC161B0   42000010   RFE                                    19.250 μs
   2281    1FC14998   0000000C   SYSCALL                                   430 ns
   2287    00000080   3C1AA000   LUI       K0,A000                         190 ns
   2903    1FC161B0   42000010   RFE                                    19.250 μs
   2923    00000080   3C1AA000   LUI       K0,A000                         630 ns
   3533    1FC1618C   42000010   RFE                                    19.060 μs
   3547    1FC1499C   0FF0586E   JAL       1FC161B8                        440 ns
   3635    00000080   3C1AA000   LUI       K0,A000                       2.750 μs


          F2                        F4         F5
         SPLIT                     MARK      DEFINE
        DISPLAY                    DATA      FORMAT
```

Figure 4-6. Subroutine display format.

Disassembly Format Definition Overlay

The Disassembly Format Definition overlay allows you to make optional display selections for the Disassembly menu and tailor it for your applications. To access this overlay, press F5: DEFINE FORMAT.

You can use this overlay to do the following:

- choose the format (mode) in which the Disassembly menu displays disassembled data

- set the interval in which the data cursor will scroll through disassembled data

- display and define the format of the timestamp

- highlight various types of disassembled cycles

- change the radix for the Address group

- choose which symbol table to use for the Address group when symbol is the selected radix

- add other groups (such as Control or Int) to the Disassembly menu display and define the radix of the groups. Setting a group's radix to Off causes the group not to be displayed.

- choose hardware or software register names for the general CPU registers

- control the choice of Big-Endian or Little-Endian mode for marking invalid bytes in data transfers, or force the data for all samples to be displayed in the Hardware display format

The Disassembly Format Definition overlay is shown in Figure 4-7.
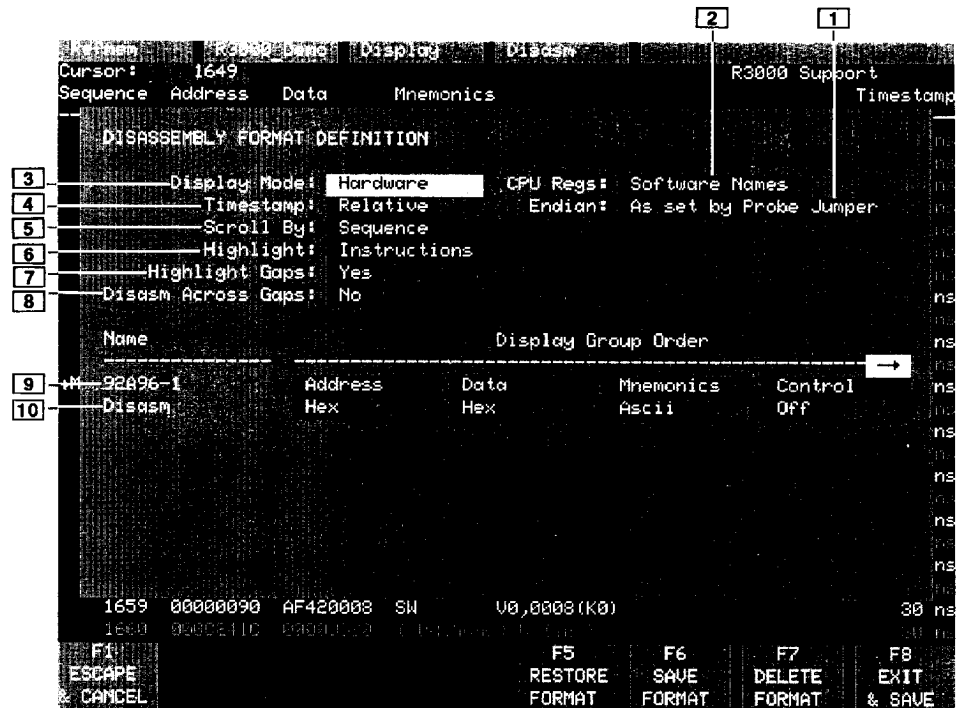
Figure 4-7. Disassembly Format Definition overlay.

[1] **Endian.** You can tell the disassembler software to use Big-Endian or Little-Endian byte ordering. You can also let the disassembler software determine the byte ordering by the position of the Big-Endian/Little-Endian jumper on the probe adapter (default selection). You can force all Data Group data to be displayed in Hardware mode by selecting Display All Data.

[2] **CPU Register Names.** You can tell the disassembler to use Software Names (default selection) or Hardware Names when displaying the CPU general purpose (integer) registers.

[3] **Display Mode.** You can display disassembled data in one of the following formats: Hardware, Software, Control Flow, or Subroutine.

[4] **Timestamp.** You can display the timestamp as an Absolute, Relative, or Delta value. You can also set the timestamp display to Off.

[5] **Scroll By.** You can scroll by Sequence, Instruction, Control Flow, or Subroutine.

[6] **Highlight.** You can highlight Instructions, Control Flow, Subroutines or all disassembled data. Highlighted data appears as white characters; non-highlighted data appears as gray characters.

7️⃣ **Highlight Gaps.** You can display or not display gaps by selecting Yes or No. Gaps are caused by qualifying data storage in the Trigger menu and appear as a gray background behind address values.

8️⃣ **Disasm Across Gaps.** You can let the software disassemble instructions across qualification gaps by selecting Yes. Selecting No will cause the software not to disassemble across gaps. Disassembling instructions across gaps associates the last sample before the gap with the sample immediately following the gap (it acts as if the gap did not exist). The disassembler assumes that a cache read missed or a conditional branch was not taken if it cannot disassemble across a gap to prove otherwise.

9️⃣ **Group Name.** You can specify the name of the display group in the column where the cursor is positioned. When you move a group, it is inserted in the new position and removed from its old position. All groups to the right of the inserted group will move one column to the right. Arrows pointing to left or right in the overlay indicate more display group columns are available but cannot be displayed on a single screen; use the left or right cursor movement keys to scroll the columns on the screen.

🔟 **Group Radix.** You can select the radix in which most groups will be displayed. The radix selections for most groups are Bin (binary), Oct (octal), Hex (hexadecimal), Sym (symbolic) and Off. The only selections for the Mnemonics group are ASCII (ASCII) and Off. The Timestamp group is always decimal and therefore has no radix field. If you select the symbolic radix, a new field appears allowing you to specify the name of the symbol table file; you cannot select a symbolic radix if you do not have any symbol tables defined.

Function Keys

F1: **ESCAPE & CANCEL.** Closes the overlay and discards any changes you have made since entering it.

F5: **RESTORE FORMAT.** Displays a list of saved disassembly formats (as well as the default format). Use the cursor keys to select the desired format to restore and press the Open/Close or Return key. If you try to restore a format that is incompatible with your module's setup, the DAS 9200 will display an error message and abort the restore operation.

F6: **SAVE FORMAT.** Saves the current selections for both the Select Options and Edit Groups functions in a file on disk. You can enter a file name up to nine characters long.

F7: **DELETE FORMAT.** Displays a list of saved disassembly formats for the current module or cluster setup. Use the cursor keys to select the desired format to delete and press the Open/Close or Return key. You cannot delete the Default format.

F8: **EXIT & SAVE.** Exits the overlay and executes or saves any changes made.

R3000 Exception Handler Entry Points

The R3000 does not perform special bus cycles during exception processing (such as vector fetches). When the disassembler detects the start of exception processing, it marks aborted opcodes as NOT EXECUTED cycles. When an exception occurs, the microprocessor saves the current program counter value in an internal register and begins execution at a predefined exception handler entry point. All hardware interrupts and software exceptions share the same exception entry point.

Table 4-1 shows the R3000 exception handler entry points. The table specifies the exception type, the virtual address, memory segment, and the physical address of the exception.

Table 4-1
Displayed Interrupt Vectors – Real Address Mode

Exception Type	Virtual Address (Hex)	Segment	Physical Address (Hex)
Reset Exception Vector	BFC0 0000	Kseg 1	1FC0 0000
UTLB Miss Exception Vector (Bev Bit = 1)	BFC0 0100	Kseg 1	1FC0 0100
UTLB Miss Exception Vector (Bev Bit = 0)	8000 0000	Kseg 0	0000 0000
General Exception Vector (Bev Bit = 1)	BFC0 0180	Kseg 1	1FC0 0180
General Exception Vector (Bev Bit = 0)	8000 0080	Kseg 0	0000 0080

Bus Cycle Types

Bus cycles are displayed according to the *R3000 System Requirements and Restrictions* described in Section 1 of this manual.

Table 4-2 describes the bus cycle types that the disassembler displays when viewing data in the Hardware format.

Table 4-2
92DM74 Bus Cycle Types

Cycle Type	Description
INST RESET	The Instruction Phase of a Reset cycle
INST MISS	An Instruction cache miss
INST FIXUP	The Instruction Phase of a Fixup cycle
NOT EXECUTED	The Instruction was fetched and then blocked from execution by exception processing. Use the Mark Opcode option to display the instruction.
INST STALL	The Instruction Phase of a Stall cycle
DATA RESET	The Data Phase of a Reset cycle
NO DATA	The Data Phase of a Run cycle with no data transfer scheduled
DATA MISS	A Data cache miss
CP TRANSFER	A data transfer between a coprocessor and the CPU. The data on the bus can be valid data.
CACHED READ	A Data read that was cached
UNCACHED READ	A Data read that was uncached
CACHED WRITE	A Data write that was cached
UNCACHED WRITE	A Data write that was uncached
WRITE INST CACHE	A Write to the Instruction Cache only
WRITE DATA CACHE	A Write to the Data Cache only
STREAMING ABORTED	The CPU dropped out of streaming after this instruction phase. The instruction will be decoded in the following fixup cycle.
DATA STALL	The Data Phase of a Stall cycle

Figures 4-8 shows an example of the Disassembly menu with some of the cycle types that can be displayed on the DAS 9200. A cached read transfer and an uncached write transfer are shown along with instruction and data cache misses and stalls.

```
Refmem            Display        Disasm
Cursor:    1361                                        R3000 Support
Sequence  Address   Data     Mnemonics                          Timestamp
--------------------------------------------------------------------------
  1346   1FC1494C  --------  ( DATA STALL )                         30 ns
  1347   1FC1494C  A0834010  SB       R3,4010(R4)                   30 ns
  1348   00000110  --------  ( DATA STALL )                         30 ns
  1349   00414950  A0834011  ( INST MISS )                          30 ns
  1350   00014010  76543210  ( CACHED READ )                        30 ns
  1351   00414954  A0434012  ( INST STALL )                         30 ns
  1352   1FC14950  --------  ( DATA STALL )                         40 ns
  1353   1FC14950  A0434012  ( INST STALL )                         20 ns
  1354   1FC14950  --------  ( DATA STALL )                         40 ns
  1355   1FC14950  A0434012  ( INST STALL )                         30 ns
  1356   1FC14950  --------  ( DATA STALL )                         30 ns
  1357   1FC14950  A0434012  ( INST STALL )                         30 ns
  1358   1FC14950  --------  ( DATA STALL )                         30 ns
  1359   1FC14950  A0434012  ( INST STALL )                         30 ns
  1360   1FC14950  --------  ( DATA STALL )                         40 ns
  1361---1FC14950--A0834011--SB--------R3,4011(R4)------------------30-ns
  1362   00014010  --------  ( DATA STALL )                         30 ns
  1363   00414954  A0434012  ( INST MISS )                          30 ns
  1364   00014010  --------  ( DATA MISS )                          30 ns
  1365   1FC14958  A0434012  ( INST STALL )                         30 ns
  1366   00014010  32------  ( UNCACHED WRITE )                     30 ns
  1367   00414958  A0434013  ( INST STALL )                         30 ns
  1368   1FC14954  --------  ( DATA STALL )                         40 ns

           F2                   F4        F5
         SPLIT                 MARK      DEFINE
        DISPLAY                DATA      FORMAT
```

Figure 4-8.   Bus cycle types in the Hardware display format

Instructions are decoded when they are fetched from cache, or in the case of a cache miss, at the end of the stall that fetches them from main memory (both instructions shown in Figure 4-8 missed in cache). Data read transfers are also displayed where they are read from cache or at the end of the stall that reads them from main memory. Data write transfers are displayed when they are first attempted; any subsequent rewrite to a busy write-buffer is displayed as a stall to avoid displaying the write data twice. Cached data reads that miss in cache are still labeled CACHED READ when their value is read from main memory (and simultaneously written to cache).

During each stall, the samples alternate between instruction phase (INST STALL) and data phase (DATA STALL). The default selections in the Custom Clock menu (described earlier in this section and in Appendix B) would have filtered out most of these samples to save acquisition memory space. The example in Figure 4-8 was taken with the clocking set to show all CPU activity.

You can display additional information about each cycle by using the Disassembly Format Definition overlay to add the Control group (in symbolic form if convenient) to the Disassembly menu.

During each Data Phase sample, non-valid bytes on the data bus are replaced with dashes (unless you selected **Display All Data** in the Endian field in the Disassembly Format Definition overlay). The disassembler determines which bytes are invalid based on the signals from the CPU and the Endian mode. If you discover that the Big/Little Endian jumper on the probe adapter was in the incorrect position when you first acquired the data, you can override the jumper setting using the Endian field in the Disassembly Format Definition overlay. The value on the data bus during Instruction phases is always shown, and makes it easier to see which samples are Instruction phases and which are Data phases.

Note that Figure 4-8 shows all data highlighted in the Disassembly menu. You can change the highlighting to highlight only control flow or subroutine instructions by changing the Highlight setting in the Disassembly Format Definition overlay.

Displaying the Address Group Symbolically

The disassembler automatically defines the radix for each displayed channel group. You can select a symbolic radix for the address group from either the Channel menu or from the Disassembly Format Definition overlay (assuming that you have a symbol table on the hard disk containing the symbolic addresses).

If you do not have any predefined symbol tables on the hard disk, you can use the Symbol Editor menu to create symbol tables in which symbols are assigned to various address ranges. Figure 4-9 shows the Address group displayed symbolically using the R3000_Addr Symbol Table file supplied with the 92DM74 software.

```
RetMem     R3000_Demo   Display     Disasm                                    
Cursor:      1305                                           R3000 Support
Sequence   Address      Data       Mnemonics                        Timestamp
                                                                          →
---------------------------------------------------------------------------
    1057   INTRP+50    10220017   BEQ     R1,R2,INTRP0              430 ns
    1071   INTRP+54    00000000   NOP                               440 ns
    1085   INTRP+58    3021203C   ANDI    R1,R1,203C                440 ns
    1099   INTRP+5C    24022000   ADDIU   R2,R0,2000                440 ns
    1113   INTRP+60    00000000   NOP                               430 ns
    1127   INTRP+64    10220040   BEQ     R1,R2,INTRP1              440 ns
    1141   INTRP+68    00000000   NOP                               440 ns
    1155   INTRP1      3C01BF80   LUI     R1,BF80                   440 ns
    1169   INTRP1+4    00000000   NOP                               430 ns
    1183   INTRP1+8    8C220010   LW      R2,0010(R1)               440 ns
    1197   INTRP1+C    8F410004   LW      R1,0004(R26)              440 ns
    1225   INTRP1+10   8F5C0070   LW      R28,0070(R26)             870 ns
    1247   INTRP1+14   8F420008   LW      R2,0008(R26)              690 ns
    1269   INTRP1+18   401A7000   MFC0    R26,EPC                   690 ns
    1291   INTRP1+1C   00000000   NOP                               690 ns
    1305   INTRP1+20   03400008   JR      R26                       430 ns
    1319   INTRP1+24   42000010   RFE                               440 ns
    1333   CACHED+4    80434013   LB      R3,4013(R2)               440 ns
    1347   UNCACH      A0834010   SB      R3,4010(R4)               440 ns
    1361   UNCACH+4    A0834011   SB      R3,4011(R4)               440 ns
    1381   UNCACH+8    A0434012   SB      R3,4012(R2)               620 ns
    1401   UNCACH+C    A0434013   SB      R3,4013(R2)               630 ns
    1421   UNCACH+10   A8434011   SWL     R3,4011(R2)               620 ns

          F2                  F4        F5
          SPLIT               MARK      DEFINE
          DISPLAY             DATA      FORMAT
```

Figure 4-9.   Address group displayed symbolically using the R3000_Demo file and the R3000_Addr symbol file.

Address Group symbol tables must use physical addresses, although this can be difficult to set up in systems actively using memory management. You should be aware that jump and branch addresses calculated by the disassembler can be incorrect if execution crosses qualification gaps or crosses memory pages that are mapped differently by the translation lookaside buffer (TLB). In such a case, the wrong address symbol can be displayed as the operand of the jump or branch.

Moving the Cursor

When displaying data in the Hardware format, you can move the cursor directly to the sequence number or enter a specific sequence number in the Cursor field in the display menu and press the Return key. In software format, some sequence numbers are suppressed. If you enter a sequence number that is suppressed, the cursor will move to the sequence nearest the suppressed sequence that can be displayed. If there is a large block of suppressed sequences near the desired sequence, there is a noticeable delay while the system searches for a sequence that can be displayed.

Marking Cycles

You can mark one or more data samples to easily identify them, to quickly move between acquisition samples, to calculate delta time stamp measurements, or to cause instructions labeled (NOT EXECUTED) or (INST MISS) to be displayed as a disassembled instruction. You can mark a data sample with an A through M, a delta mark (Δ), or force disassembly of a bus cycle using the Mark Data feature of the Disassembly menu. The letter "m" is placed next to any sample that has been disassembled by being marked with an opcode mark.

You can use both data and opcode marks on a data sample. However, you cannot force disassembly of a bus cycle that is not an instruction phase. You can also undo opcode marks on any previously marked instruction phase.

Manually Overriding Disassembled Instructions

The 92DM74 disassembler software labels instructions as (NOT EXECUTED) when it determines that the instruction was prevented from completing its execution due to the start of exception processing. The disassembler also defaults to marking instruction cache reads as (INST MISS) if it cannot scan past a qualification gap or the end of the acquisition memory to prove that a cache read was successful. Sometimes you need to force these bus cycles to be displayed as decoded instructions to see what was actually fetched.

To force any instruction phase sequence to be decoded as an instruction, you can use F4: MARK DATA to mark the sequence with an opcode mark. You can then remove the mark using the Undo Mark selection in the Mark Data window if necessary. The disassembler will not let you change non-instruction phase samples (such as reads or writes); if you place the cursor on these sequences, the Opcode and Undo Mark selections will not appear in the Mark Data window (the data phase samples are controlled by selecting the contents of the Endian field in the Disassembly Format Definition overlay).

To use the Mark Opcode function to disassemble an instruction phase, follow these steps:

1. Place the cursor on the sequence you want to change in the Disassembly menu.

2. Press F4: MARK DATA, the Mark Data window appears containing a list of Mark Data selections. The contents of the list will vary from sample to sample to reflect logical opcode or mark data selections for that sample. Unlike data marks that can only be used for one sample at a time, opcode marks can be used as often as necessary.

3. Press the Return or Open/Close key to mark the opcode.

   The data sample will change to match the selected opcode mark; the selection has no effects on other samples. The disassembler places the letter "m" to the left of the sample indicating that you have marked the sample.

Figure 4-10 shows an example of an instruction that has been disassembled and displayed after using the F4: MARK DATA key to place an opcode mark on sequence 703. Prior to marking, the instruction was labeled (NOT EXECUTED) because the start of exception processing, three instructions later, blocked it from executing in the instruction pipeline writeback stage (the disassembler checks for Excl W*). The instruction is now marked with an "m" (at left edge of the screen).

The Mark Opcode function can be particularly useful to determine the reason for some exceptions (such as those involving address errors). In such cases, the instruction is blocked from execution and marked (NOT EXECUTED) by the exception that it caused.

Marking an instruction that is already correctly decoded, such as (RESERVED), has no effect other than to place the letter "m" at the left margin of the screen.

```
Refmem      R3000 Demo   Display    Disasm
Cursor:    703                                    R3000 Support
Sequence  Address     Data      Mnemonics                                      Timestamp
                                                                                   →
T    511  LOOP———————00000000—NOP——————————————————————————————————————————————440—ns
     525  LOOP+4      AC434000  SW        R3,4000(R2)                            440 ns
     539  LOOP+8      3C037654  LUI       R3,7654                                440 ns
     557  LOOP+C      34633210  ORI       R3,R3,3210                             560 ns
     571  LOOP+10     00000000  NOP                                              440 ns
     585  LOOP+14     AC434010  SW        R3,4010(R2)                            430 ns
     599  LOOP+18     00000000  NOP                                              440 ns
     617  BYTE        3C04A000  LUI       R4,A000                                560 ns
     631  BYTE+4      00822025  OR        R4,R4,R2                               440 ns
     645  BYTE+8      80834010  LB        R3,4010(R4)                            440 ns
     659  BYTE+C      80834011  LB        R3,4011(R4)                            440 ns
     681  CACHED      80434012  LB        R3,4012(R2)                            680 ns
m    703—CACHED+4—————80434013—LB—————————R3,4013(R2)————————————————————————————690—ns
     705  0041494D    A0834010  ( NOT EXECUTED )                                 70 ns
     707  00414950    A0834011  ( NOT EXECUTED )                                 60 ns
     709  GEN_VEC0    3C1AA000  LUI       R26,A000                               60 ns
     711  GEN_VEC0+4  275A2418  ADDIU     R26,R26,2418                           60 ns
     713  GEN_VEC0+8  AF410004  SW        R1,0004(R26)                           60 ns
     715  GEN_VEC0+C  AF5C0070  SW        R28,0070(R26)                          70 ns
     717  GEN_VEC+10  AF420008  SW        R2,0008(R26)                           60 ns
     719  GEN_VEC+14  24020001  ADDIU     R2,R0,0001                             60 ns
     727  GEN_VEC+18  3C019FC1  LUI       R1,9FC1                                250 ns
     735  GEN_VEC+1C  24216000  ADDIU     R1,R1,6000                             250 ns
               F2                   F4        F5
              SPLIT                MARK      DEFINE
             DISPLAY               DATA      FORMAT
```

Figure 4-10. Marked opcode. The marked sample at sequence 703 was
previously labeled as (NOT EXECUTED). The instruction was
decoded and displayed using the Mark Opcode function with the
F4: MARK DATA key. In this example, the instruction is a
Load Byte instruction (rather than a LH or LW instruction) and
is not responsible for the exception that follows.

Marking a Data Sample

You can mark all samples to easily identify them and to quickly
move the cursor to a marked sample. A special mark, the delta
mark (∆), is used to calculate delta timestamp values.

The available marks are the letters A through M and ∆. When
you mark a data sample, that mark is attached to the acquired
data. The mark will appear with the data sample in all other
display menus until you change it. If you view data in a split-
screen display, the mark is attached only to the window in which
it is placed and is not carried over to the other window.

A small arrow appears at the beginning of the line of the marked
data sample to make the mark more visible. The arrow
disappears when both a data mark and an opcode mark are
placed on the same sample. You can place more than one mark
on a data sample; however, only one of the marks will be visible.

To place a mark on a data sample, follow these steps:

1. Place the cursor on the data sample you want to mark in the Disassembly menu.

2. Press F4: MARK DATA and select a mark (letters A through M and Δ).

    When you press F4: MARK DATA, a list of selections appears. The cursor in the selection list will always be on the next unused mark (unless there are opcode marks available for the sample). If you select a mark that has already been used, the previously marked sample will be unmarked and the current sample will be labeled with that mark when you close the selection list. Each mark can only be used on one data sample.

3. Press the Return or Open/Close key.

You can use the Δ mark to make delta timestamp measurements. After placing a Δ mark on a data sample, you can select the Delta selection in the Timestamp field of the Disassembly Format Definition overlay. When you press F8: EXIT & SAVE, the Disassembly menu samples will show the time elapsed between the data sample with the Δ and each previous and subsequent sample.

To quickly move from one data mark to another, type the mark in the Cursor field.

Searching Through Data

The 92DM74 disassembler does not have a Disassembly Search Definition overlay. To search through disassembled data you can use the Split-Screen function of the DAS 9200 to link the Disassembly menu to the State menu. You can then search for data using parameters you specify in the State Search Definition overlay as outlined in your module user's manual. To set up the split-screen display, use the following procedure:

1. Press F2: SPLIT DISPLAY to access the Split-Screen overlay.

2. Select the State menu for one half of the split-screen display and the Disassembly menu for the other half.

3. Press F5: SPLIT HORIZ to split the display into two horizontal displays. You can also split the display into two vertical displays by pressing F6: SPLIT VERT.

4. Press F2: LOCK CURSORS. A new window appears so you can lock the cursors to the same sequence, or to the current position.

5. Select **lock cursors at the same sequence** and press the Return key.

6. Press F8: EXIT & SAVE to save the changes to the overlay and to display the split-screen.

7. If the active menu (the menu with the yellow cursor and yellow cursor field) is the Disassembly menu, press F3: SWITCH WINDOW to make the State menu the active menu.

8. Press F6: DEFINE SEARCH and specify the search parameters in the State Search Definition overlay.

9. Press F8: EXIT & SAVE to save the search parameters.

10. Press F7: SEARCH BACKWARD or F8: SEARCH FORWARD to execute the search function. The DAS 9200 will begin searching for the desired data. When the DAS 9200 finds the data, the cursors in both menus will identify the acquisition sequence containing the search pattern.

11. To abort a search operation, press the Esc (Escape) key.

Figure 4-11 shows an example of the split-screen display with the cursors locked on the same sequence.

Figure 4-11. State and Disassembly split-screen display used to perform searches.

PRINTING DATA

To print disassembled data, use the Disassembly Print overlay. To access this overlay, press the Shift and Print keys at the same time from the Disassembly menu.

You can choose one of two destinations for the disassembled data: the RS-232 Auxiliary Port or a file stored on the hard disk. The data is formatted the same in both cases. Appendix C in the *DAS 9200 System User's Manual* contains information on connecting the RS-232 Auxiliary Port to a printer.

If the Send Output To field is set for a file, you need to name the file (the default name is Output). The file is stored in the Print Output directory. This file can then be renamed, deleted, copied to a floppy disk, and so on from the Disk Services menu.

If the Send Output To field is set for the RS-232 Auxiliary port, the printer attached to this port receives the data for printing. To set the rate of transmission (baud rate) for the Auxiliary port, select the Communications menu and set the baud rate to match the data rate of your printer.

The parameters you can define in the Disassembly Print overlay are as follows:

- characters per line
- lines per page
- spaces to indent
- new line characters
- new page characters
- comment for page headings
- print the Disassembly Format Definition overlay

Printed data looks similar to the data displayed on a DAS 9200 terminal screen.

If the width of the data exceeds the width of the specified line length (maximum 300 characters), greater than symbols (>) are printed to indicate that the data continues past the edge of the page. If you define more characters per line than can fit on a page, the data will either print on the next line or run off the edge of the page, depending on the type of printer being used. To print the display screen, make the appropriate selections for the Saved Printer Settings (top of the Disassembly Print overlay) and the output specification, and press F5: PRINT.

During printing, you can abort the printing sequence at any time by pressing F5: STOP PRINT.

NOTE

The DAS 9200 does not detect printer errors and will not give any error or warning messages if the print sequence cannot be completed.

For information on printer cable connections, refer to Appendix C in your DAS 9200 System User's Manual.

Figure 4-12 shows the Disassembly Print overlay.
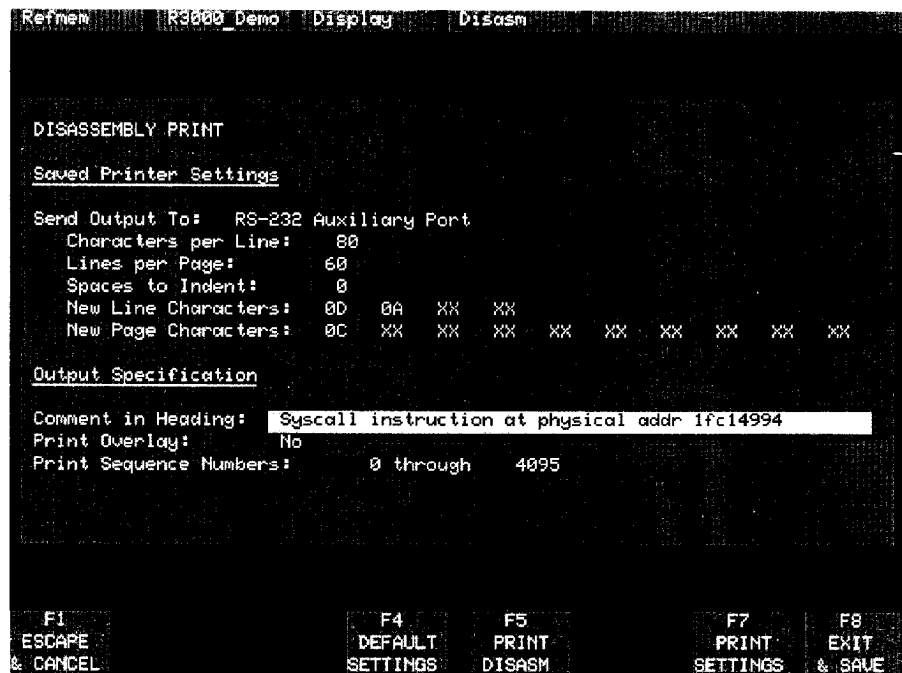
Figure 4-12. Disassembly Print overlay.

Section 5: HARDWARE ANALYSIS

You may need to perform hardware analysis on your R3000 system prior to, during, and after attempting to integrate your software with the R3000 system hardware. You can view acquired data with the State or Timing menus depending on your needs. To verify if you are acquiring specific bit patterns, you can use the State menu. To perform timing analysis, it makes more sense to view acquired data using the predefined timing formats supplied with the 92DM74 software.

The 92DM74 software provides you with two different ways to perform hardware analysis. To perform a quick hardware analysis, you can use the State or Timing menus with the setups provided by the 92DM74 disassembly software. To perform a more detail timing analysis, you can use a predefined setup (R3K_Timg_A96) provided for you with the 92DM74 software. This section discusses hardware analysis using both of these methods.

R3000 SUPPORT HARDWARE ANALYSIS

The 92A96 Module acquires data from 96 channels including 15 signals that are not necessary for mnemonic disassembly. Some of these 15 signals are meaningful in disassembly and others are only useful for hardware analysis. Appendix B contains a description of these signals and how they can be useful.

If you are not interested in acquiring data from these signals, you can disconnect them from the probe adapter and reconnect the channels (podlets) to other system signals more useful to you. Refer to *Alternate Connections* in Section 3 for information on which channels you can use to make alternate connections between the DAS 9200 and the system under test. Refer to *Removing and Replacing Podlets* in Appendix C for information on separating the individual podlets from an 8-channel probe.

NOTE

Because the podlet ground connector represents approximately 300 Ω to ground, it is recommended that you use extreme care or, preferably, power down your R3000 system before making alternate connections. Power on your R3000 system after all connections are made. It is not necessary to power down the DAS 9200.

If you are not switching between the Disassembly and State or Timing menus, you can use any channel (except the clock and qualifier channels) to make alternate connections. You can only move the eight clock/qualifier channels if you do not use custom clocking. If you move any channels that are part of a display group where a symbol table is defined, the symbol table will no longer be accurate.

Clocking

To change the data sampling rate, use the Clock menu. The clock menu is shown in Figure 4-1. The default clocking mode is Custom when you use the R3000 microprocessor support. To perform hardware analysis, you will want to use the Internal or External clocking modes. The Internal clock selection can sample data up to 100 MHz on all 96 channels, which has a 10 ns resolution between samples. The External clock selection samples data on every active clock edge on the 92A96 clock inputs up to 100 MHz. Refer to your your acquisition module user's manual for specific details on the Clock menu.

Internal Clocking

When you select Internal as the clocking mode, the data acquisition module stores one data sample as often as every 10 ns (100 MHz). This clocking selection is commonly referred to as asynchronous.

Two typical uses of Internal clocking might be to verify that all the R3000 signals are transitioning as expected or to measure the timing relationship between signals.

It is possible to acquire asynchronous data at rates of 200 MHz and 400 MHz. The faster the 92A96 Module acquires data, the fewer channels it can acquire data on. A single 92A96 Module can acquire data on 24 channels at 400 MHz or 2.5 ns resolution. Refer to your *92A96 Module User's Manual* for information on sampling data at speeds faster than 100 MHz.

External Clocking

When you select External as the clocking mode, the data acquisition module acquires and stores data based on the clock channel up to 100 MHz. This clocking selection is commonly referred to as synchronous.

By selecting the rising edge of any of the available clocks on the data acquisition module as the clock channel, and turning off the remaining three clocks, the data acquisition module will sample data on every rising edge of the selected clock. No data is acquired on the falling clock edge unless you select both edges.

Triggering

All the Trigger menu selections currently available for your data acquisition module are still valid for disassembly. Refer to your module user's manual for a list and description of the selections.

NOTE

The R3000 Trigger Library selection called R3000_Lib and the Control group symbol table will normally be inappropriate for triggering when using Internal or External Clocking; they are designed to work with Custom Clocking only.

Acquiring Data

You can acquire data as described in the *Acquiring Data* description in Section 4.

Displaying Data

Hardware analysis requires that you view data in either the State or Timing menus. In the State menu, all channel group values are shown based on the selected radix in the Channel menu or the State Format Definition overlay; no instruction mnemonics are displayed. In the Timing menu, every channel is shown as a waveform.

A predefined Timing Format Definition overlay file, part of the R3000 microprocessor support, is available for you to use when displaying data in the Timing format. The R3000_96 file was installed on the DAS 9200 with the disassembler software, and is used with data acquired by the disassembler (that is, with the channel grouping as defined by the R3000 Microprocessor Support).

This timing format places the Address and Data groups as bus forms on the first two lines followed by a synthesized signal called Phase. The Phase signal is normally a buffered DClk signal unless the caches are swapped; then it becomes IClk. These signals are followed by other important control signals.

To select the R3000_96 file, follow these steps:

1. Select the Timing menu and press F5: DEFINE FORMAT.

2. Press F5: RESTORE FORMAT.

3. Select R3000_96 and press the Return key. A message tells you the format file is selected.

4. Press F8: EXIT & SAVE to return to the Timing menu.

Timing data is now displayed in the format described above.

R3000 TIMING ANALYSIS

Data acquired by the disassembler is not optimal for hardware analysis because the probe adapter circuitry latches and stretches selected signals to help disassemble and trigger on cycle types. In addition, the disassembler groups parts of the R3000 microprocessor's Tag and AdrLo bus to form a single address group. To assist in hardware analysis or timing analysis, the probe adapter provides a Timing/Normal jumper to bypass the additional latching and stretching of certain signals. Also, the software provides a separate module setup file called R3K_Timg_96 which acquires the Tag and AdrLo signals in two separate channel groups, and defines alternate smaller groups of clock and control channels. A predefined Timing Format Definition overlay file, also called R3K_Timg_96 (with bus forms), is used to view this data.

Restoring the R3K_Timg_96 Setup File

When you restore the R3K_Timg_96 setup file, the DAS 9200 switches the 92A96 Module from the R3000 microprocessor support to the General Purpose Support for the hardware analysis. You cannot perform disassembly on the acquired data. If you want to perform disassembly on the acquired data, you need to reselect the R3000 Support in the Configuration menu.

To restore the R3K_Timg_96 setup, follow these steps:

1. From the Menu Selection Overlay, select Save/Restore from the Utilities column, and press F6: MOVE TO UTILITY.

2. Move the cursor to the File field in the Save/Restore menu and select the R3K_Timg_96 setup file.

3. Press F8: EXECUTE OPERATION to restore the setup.

4. If you have not already done so, move the Timing/Normal jumper on the probe adapter to the Timing position.

The DAS 9200 sets up the individual setup menus according to the contents of the R3K_Timg_96 setup file. Table 5-1 (listed at the end of this section) shows the channel assignments for the R3K_Timg_96 setup file. The following paragraphs describe the setups for some of the setup menus.

Clocking

To perform hardware analysis, you will want to use the Internal or External clocking modes. Refer to your your acquisition module user's manual for specific details on the Clock menu.

If you use Internal clocking and one of the High-Speed Timing modes, you will usually need to move the podlets to the appropriate connectors on the probe adapter. Refer to Table 5-1 for a list of the 92A96 channels and their associated signals.

When you acquire synchronous data from your R3000 system, the recommend External Clock selection is the OR of the falling edges of IClk (Clock 3) and DClk (Clock 2). You can also use the other two clock channels as qualifiers or clocks to further modify clocking for your R3000 system.

Note that when you use the External Clocking as described earlier, virtually the same data will be acquired as with the least explicit Custom Clocking selection. The main difference is that the data is not pipelined (that is, address and corresponding data is not in the same acquisition sample). This lets you acquire and disassemble basically the same data as acquired using Internal or External clocking.

Triggering

All the Trigger menu selections currently available for your data acquisition module are still valid for disassembly. Refer to your module user's manual for a list and description of the selections.

Acquiring Data

You can acquire data as described in the *Acquiring Data* description in Section 4.

Displaying Data

Hardware analysis requires that you view data in either the State or Timing menus. The following discussion describes these menus.

State Menu

In the State menu, all channel group values are shown based on the selected radix in the Channel menu or the State Format Definition overlay. No instruction mnemonics are displayed. Refer to Table 5-1 or C-4 for a complete list of acquired signals by individual channel groups. Figure 5-1 shows data sampled with External clocking in the State menu.

Refmem	R3K_Timg_9	Display	State			
Cursor:	148	T				
Sequence	Tag AdrLo	Data	Clks	CacheCtl	Sys_Ctrl	Int
137	0000 609C	00000000	00	11101	01111011111	37
138	0000 609C	00000000	01	01111	01111011111	37
139	0000 609C	00000000	11	01111	01111011111	37
140	0000 02C0	20002014	10	01111	01111011111	37
141	0000 02C0	20002014	00	01111	01111011111	37
142	0000 0001	00000004	00	01101	01111111111	37
143	0000 02BC	00000000	01	01111	11101011111	37
144	0000 02BC	00000000	11	01111	11101011101	37
145	0001 02BC	00000000	10	11111	11101011101	37
146	0001 02BC	00000000	00	11111	11101011101	37
147	0001 02BC	00000000	00	11111	11101011101	37
◆A 148	0001—02BC	00000000	01	11111	11101011101	37
149	0001 02BC	00000000	01	11111	11101011101	37
150	0001 02BC	00000000	00	11111	11101011101	37
151	0001 02BC	00000000	10	11111	11101011101	37
152	0001 02BC	00000000	10	11111	11101011001	37
153	0001 02BC	00000000	11	11111	11101011001	37
154	0001 02BC	00000000	01	11111	11101011001	37
155	0001 02BC	00000000	00	11111	11101011001	37
156	0001 00BC	00000000	10	11111	10101011001	37
157	0001 609C	346302C8	10	11111	10001011001	37
158	0001 609C	346302C8	11	11111	11011011011	37
159	0001 629C	346302C8	01	11111	11111011011	37

	F2		F4	F5	F6	F7	F8
	SPLIT DISPLAY		MARK DATA	DEFINE FORMAT	DEFINE SEARCH	SEARCH BACKWARD	SEARCH FORWARD

Figure 5-1.   State data acquired with the R3K_Timg_96 setup.

Timing Menu

In the Timing menu, every channel is shown as a waveform.

A predefined Timing Format Definition overlay file, part of the R3000 microprocessor support using the R3K_Timg_96 setup, is available for you to use when displaying data in the Timing format. The R3K_Timg_96 file was also installed on the DAS 9200 with the disassembler software (the module setup file uses the same name as the timing format file and a demonstration reference memory).

This timing format displays the Tag and AdrLo groups as separate bus forms and reorganizes the control signals to make them more suitable for timing analysis.

To select the R3K_Timg_96 file, follow these steps:

1. Select the Timing menu and press F5: DEFINE FORMAT.

2. Press F5: RESTORE FORMAT.

3. Select R3K_Timg_96 and press the Return key. A message tells you the format file is selected.

4. Press F8: EXIT & SAVE to return to the Timing menu.

Timing data is now displayed in the format described above.

Figure 5-2 shows data displayed using the R3K_Timg_96 Timing Format file.
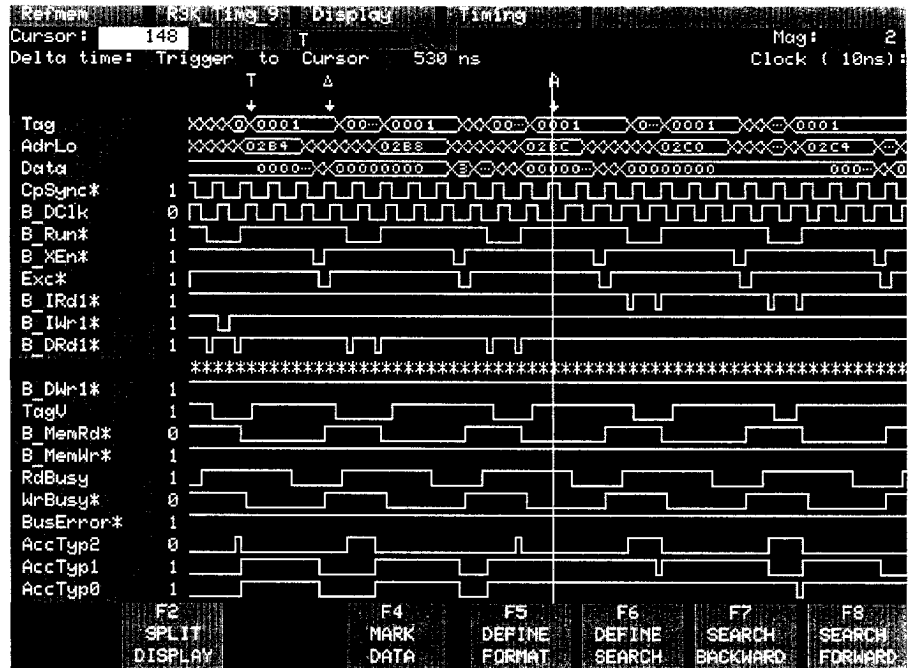
Figure 5-2. Timing data displayed using the R3K_Timg_96 Timing Format file.

Table 5-1
Channel Assignments for the R3K_Timg_96 Setup file

92DM74 Group (Radix)	Group Bit Pos	92A96 Section Channel	Voltage Threshold, Polarity	R3000/A Signal Name	PGA
Tag (Hex)	15	A3: 7	TTL, +	Tag31	L14
	14	A3: 6	TTL, +	Tag30	L15
	13	A3: 5	TTL, +	Tag29	J14
	12	A3: 4	TTL, +	Tag28	J13
	11	A3: 3	TTL, +	Tag27	K15
	10	A3: 2	TTL, +	Tag26	J15
	9	A3: 1	TTL, +	Tag25	H14
	8	A3: 0	TTL, +	Tag24	H15
	7	A2: 7	TTL, +	Tag23	F15
	6	A2: 6	TTL, +	Tag22	G14
	5	A2: 5	TTL, +	Tag21	F14
	4	A2: 4	TTL, +	Tag20	E14
	3	A2: 3	TTL, +	Tag19	D15
	2	A2: 2	TTL, +	Tag18	C15
	1	A2: 1	TTL, +	Tag17	D14
	0	A2: 0	TTL, +	Tag16	E13
AdrLo (Hex)	15	A1: 7	TTL, +	AdrLo15	A7
	14	A1: 6	TTL, +	AdrLo14	A6
	13	A1: 5	TTL, +	AdrLo13	B7
	12	A1: 4	TTL, +	AdrLo12	B5
	11	A1: 3	TTL, +	AdrLo11	A4
	10	A1: 2	TTL, +	AdrLo10	A3
	9	A1: 1	TTL, +	AdrLo9	B4
	8	A1: 0	TTL, +	AdrLo8	C5
	7	A0: 7	TTL, +	AdrLo7	B3
	6	A0: 6	TTL, +	AdrLo6	A2
	5	A0: 5	TTL, +	AdrLo5	C4
	4	A0: 4	TTL, +	AdrLo4	C2
	3	A0: 3	TTL, +	AdrLo3	B1
	2	A0: 2	TTL, +	AdrLo2	D2
	1	A0: 1	TTL, +	AdrLo1	E3
	0	A0: 0	TTL, +	AdrLo0	C1
Data (Hex)	31	D3: 7	TTL, +	Data31	Q4
	30	D3: 6	TTL, +	Data30	P8
	29	D3: 5	TTL, +	Data29	Q7
	28	D3: 4	TTL, +	Data28	Q5
	27	D3: 3	TTL, +	Data27	P6
	26	D3: 2	TTL, +	Data26	P5
	25	D3: 1	TTL, +	Data25	Q3
	24	D3: 0	TTL, +	Data24	N5

(Cont.)

Table 5-1 (Cont.)
Channel Assignments for the R3K_Timg_96 Setup file

92DM74 Group (Radix)	Group Bit Pos	92A96 Section Channel	Voltage Threshold, Polarity	R3000/A Signal Name	PGA
	23	D2: 7	TTL, +	Data23	P1
	22	D2: 6	TTL, +	Data22	P4
	21	D2: 5	TTL, +	Data21	Q2
	20	D2: 4	TTL, +	Data20	P2
	19	D2: 3	TTL, +	Data19	N3
	18	D2: 2	TTL, +	Data18	N2
	17	D2: 1	TTL, +	Data17	L3
	16	D2: 0	TTL, +	Data16	M2
	15	D1: 7	TTL, +	Data15	K1
	14	D1: 6	TTL, +	Data14	N1
	13	D1: 5	TTL, +	Data13	M1
	12	D1: 4	TTL, +	Data12	L2
	11	D1: 3	TTL, +	Data11	K2
	10	D1: 2	TTL, +	Data10	J1
	9	D1: 1	TTL, +	Data9	J3
	8	D1: 0	TTL, +	Data8	H3
	7	D0: 7	TTL, +	Data7	F2
	6	D0: 6	TTL, +	Data6	H1
	5	D0: 5	TTL, +	Data5	H2
	4	D0: 4	TTL, +	Data4	G1
	3	D0: 3	TTL, +	Data3	G2
	2	D0: 2	TTL, +	Data2	F3
	1	D0: 1	TTL, +	Data1	D1
	0	D0: 0	TTL, +	Data0	E2
Clks (Bin)	1	C3: 2	TTL, +	B_DClk¶	P11
	0	C1: 7	TTL, +	CpSync*	Q14
CacheCtl (Bin)	4	C0: 6	TTL, +	TagV	N15
	3	C3: 6	TTL, +	B_IRd1*,†	P12
	2	C3: 5	TTL, +	B_IWr1*,†	P13
	1	C3: 4	TTL, +	B_DRd1*,†	N11
	0	C2: 5	TTL, +	B_DWr1*,†	Q14
Sys_Ctrl	10	C2: 3	TTL, +	B_Run*,†	N14
(Bin)	9	C2: 2	TTL, +	B_XEn*,†	P7
	8	C2: 6	TTL, +	Exc*	Q8
	7	C2: 1	TTL, +	B_MemRd*,†	N13
	6	C2: 0	TTL, +	B_MemWr*,†	N12
	5	C3: 7	TTL, +	AccTyp2	L13
	4	C3: 3	TTL, +	AccTyp1	M14
	3	C2: 7	TTL, +	AccTyp0	P15
	2	C2: 4	TTL, +	RdBusy	C11
	1	C3: 0	TTL, +	WrBusy*	A13
	0	C1: 1	TTL, +	BusError*	B12

(Cont.)

Table 5-1 (Cont.)
Channel Assignments for the R3K_Timg_96 Setup file

92DM74 Group (Radix)	Group Bit Pos	92A96 Section Channel	Voltage Threshold, Polarity	R3000/A Signal Name	PGA
Int (Hex)	5	C0: 5	TTL, +	Int*(5)	A12
	4	C0: 4	TTL, +	Int*(4)	C10
	3	C0: 3	TTL, +	Int*(3)	B10
	2	C0: 2	TTL, +	Int*(2)	A11
	1	C0: 1	TTL, +	Int*(1)	B9
	0	C0: 0	TTL, +	Int*(0)	C9
CP_Ctl (Off)	4	C1: 0	TTL, +	CpBusy	B11
	3	C1: 5	TTL, +	CpCond3	A10
	2	C1: 4	TTL, +	CpCond2	A9
	1	C1: 3	TTL, +	CpCond1	B8
	0	C1: 2	TTL, +	CpCond0	A8
Misc (Off)	2	C3: 1	TTL, +	Reset*	A14
	1	C0: 7	TTL, +	DRW_Fixup*=	‡
	0	C1: 6	TTL, +	Endian	§

¶ Buffered signal; unbuffered signal is available on a square pin (labeled CK2) on the probe adapter
† Buffered signals, unbuffered signals not available on the probe adapter
‡ DRW_Fixup*= is a synthesized signal on the probe adapter
§ Defined by Big/Little Endian jumper on the probe adapter

SEARCHING THROUGH DATA

You can view and search through data as described in the *Searching Through Data* description in Section 4.

PRINTING DATA

You can print state data as described in the *Printing Data* discussion in Section 4. To access this overlay, press the Shift and Print keys at the same time from the State menu.

To print timing data, use the Timing Print overlay. To access this overlay, press the Shift and Print keys at the same time from the Timing menu.

For detailed information on the State Print overlay or the Timing Print overlay, refer to your module user's manual.

Appendix A:
ERROR MESSAGES AND DISASSEMBLY PROBLEMS

This section describes error messages and disassembly problems that you may encounter while acquiring data.

MODULE ERROR MESSAGES

These error messages will appear in the Module Monitor menu when there are problems with acquiring data or satisfying the trigger program. The error messages are listed in alphabetical order; a description of the error message and the recommended solution follow the error message.

Slow Clock

This message appears when acquisition records are not occurring or are typically occurring at 1 ms or slower intervals possibly due to one of the clock signals or one of the clock qualifiers. Check for the following:

1. The R3000 system is powered on and running. Be sure the system is not halted.

2. R3000 Support is selected in the 92A96 Configuration menu.

3. Custom is selected in the Clock menu.

4. The clock and 8-channel probe connections between the interface housings and probe adapter are correct (clock, section names, and channel numbers match), are properly oriented (GND connects to ground), and are fully engaged.

5. The connections between the interface housings and 92A96 probe cables have matched color labels, matched slot numbers, and are properly keyed.

6. The connections between the 92A96 probe cables and probe connectors have matched color labels, matched slot numbers, and are properly keyed.

7. The orientation of pin A1 on the R3000 in the probe adapter is correct.

8. The lever on the ZIF socket is down and locked.

9. The orientation of pin A1 on the probe adapter in the R3000 system is correct.

10. No bent or missing pins on the microprocessor or on either of the probe adapter sockets.

11. The Normal/Timing jumper on the probe adapter is in the Normal position.

Waiting for Stop

This message appears when the trigger condition is satisfied and memory is full but the Manual Stop mode is selected in the Cluster Setup menu. The solution is to manually stop the DAS 9200 by pressing F1: STOP.

This message can also appear when other modules in the cluster have not filled their memories. Wait for the other modules to fill their memories. If the message does not disappear in a short time, press F1: STOP.

Waiting for Stop-Store

This message appears when the trigger condition is satisfied but the amount of post-fill memory specified in the trigger position field is not yet filled. Press F1: STOP to view the acquired data, then check for the following:

1. The trigger program in the Trigger menu is correct.

2. The storage qualification in the Trigger menu is correct.

3. The system or the module does not have an exception or fault and is not in a continuous Multiprocessor Stall. The R3000 system or data acquisition module might have experienced a hardware or software exception or fault after the trigger condition was satisfied or may have been stalled by another device.

Waiting for Trigger

This message appears when the trigger condition doesn't occur. Check for the following:

1. The R3000 system is powered on and running. Be sure the system is not halted or stalled.

2. The trigger conditions are not being satisfied. The Module Monitor menu shows which state the trigger machine is in and the current value of the counter/timers. Press F1: STOP, access the Trigger menu, and redefine the conditions for that state. Also refer to the description on *Triggering* in Section 4.

DISASSEMBLER ERROR MESSAGES

Disassembler error messages appear in the Disassembly menu when there are problems acquiring disassembled data. If there is more than one error message, a window appears containing the list of error messages. If there are more error messages than can be displayed in the window, you can use the Return key to page to the other messages. To close the error message window, press the Esc (escape) key. The disassembler always tries to recover an error and displays the action taken to remedy the problem. There are occasions when you need to make other changes to remedy the problem to override the disassembler's recovery actions.

OTHER DISASSEMBLY PROBLEMS

There may be problems with disassembly for which no error messages are displayed. Because the disassembler acquires physical translated addresses, sometimes it can calculate the target address of a jump or branch instruction incorrectly if the execution crosses two differently mapped memory pages.

Other problems and their recommended solutions follow.

Incorrect Data   If the data acquired is obviously incorrect, check the following:

1. R3000 Support is selected in the 92A96 Configuration menu.

2. The Normal/Timing jumper is in the Normal position.

3. The Big/Little Endian jumper is in the correct position.

4. The clock and 8-channel probe connections between the interface housings and probe adapter are correct (clock, section names, and channel numbers match), are properly oriented (GND connects to ground), and are fully engaged.

5. The connections between the interface housings and 92A96 probe cables have matched color labels, matched slot numbers, and are properly keyed.

6. The connections between the 92A96 probe cables and probe connectors have matched color labels, matched slot numbers, and are properly keyed.

7. The orientation of pin A1 on the R3000 in the probe adapter is correct.

8. The lever on the ZIF socket is locked.

9. The orientation of pin A1 on the probe adapter in the R3000 system is correct.

10. No bent or missing pins on the microprocessor or on either of the probe adapter sockets.

Other Suggestions   If the previous suggestions don't fix the problem with acquiring disassembled bus cycles or instruction mnemonics, try the following:

1. Reload the module setup by selecting the R3000 Support in the 92A96 Configuration menu to restore the DAS 9200 to known state.

2. Possible ac and dc loading problems may be remedied by removing the ZIF socket from the probe adapter. If this doesn't ease the loading problem sufficiently, you should remove one or both of the protective sockets from the probe adapter. However, it may not be possible to remove both sockets since the probe adapter is designed to support the 145- and 175-pin packages. These sockets may add enough additional inductance to your R3000 system to affect it.

    If your system uses the R3000A microprocessor instead of the R3000, you should use the 175-pin socket on the probe adapter. Refer to Appendix C for a description to remove sockets from the probe adapter.

3. System timing can require that the custom clocking be restricted to the two choices that include all stall phases. Refer to *Supplemental Timing Information* in Appendix B for information on the timing requirements.

If the DAS 9200 still is not acquiring data after trying these solutions, there may be a problem with your R3000 system. Try performing hardware analysis with your DAS 9200 system to ensure that the R3000 signals are valid at the time the probe adapter samples them.

Refer to *Section 5: Hardware Analysis* for information on data sampling rates using either the Internal or External clocking selections in the Clock menu. Also refer to *Appendix B: How Data is Acquired* to see when the disassembler samples the various R3000 system signals.

Appendix B:
HOW DATA IS ACQUIRED

This appendix provides detailed information on how data is acquired using Custom Clocking and provides additional information on signals acquired for disassembly and those signals not acquired.

92A96 CUSTOM CLOCKING

Instruction and Data Bus Transfers. The R3000 external buses are a multiplexed Harvard architecture. Instruction and Data bus transfers are multiplexed onto a single set of pins. Individual bus transfers are defined as phases. IClk and DClk are used by the 92DM74 to acquire R3000 data; the active falling edge used in a particular phase is indicated with a dash in Figure B-1. IClk is used to acquire Data Phases while DClk is used to acquire Instruction Phases. An Instruction and Data Phase together compose a cycle, which corresponds to one R3000 clock cycle. This results in a maximum bus cycle rate of twice the microprocessor's clock rate.

In Figure B-1, the Data and Instruction Phases where signals are valid is identified with the letters D and I. The numbers next to D and I indicate when the 92DM74 Master Clock samples the R3000 signals and stores them into the 92A96 Module's acquisition memory as a complete data acquisition record. The 92DM74 also uses the 92A96 Module's proprietary de-pipelining circuitry to sample and time-align address, data and control into one complete data acquisition record. This simplifies triggering by making it possible to trigger on a complete bus cycle using a single trigger word.

The 92A96 Module's sophisticated clocking state machine also builds a complete bus cycle for Instructions and Data Phases for both cache and memory transfers. During cache transfers, the address information is presented and removed one phase earlier than the data transfer. For an Instruction Phase, the address is provided during the previous Data Phase. During the Instruction Phase, the cache control signals are asserted and the data bus is sampled; if a data transfer is scheduled for the next Data phase, the data address is also placed on the address bus.

Main Memory Transfers. In addition to cached transfers, the R3000 performs main memory transfers. The main memory transfers primarily consist of reads and writes to the main memory using control signals to implement a handshake protocol to support the various device speeds. When accessing slow devices, the R3000 performs a series of Stall cycles to wait for the devices's access time to be satisfied. Therefore, instruction and data cache misses or uncached transfers are performed using Stall cycles which require a minimum of two clock cycles.

Setup and Hold Requirements. To satisfy the 92A96 Module's setup and hold requirements, the MemRd*, MemWr*, IRd*, DRd*, Run* and XEn* signals are latched and stretched; the IWr* and DWr* signals are buffered through circuitry on the probe adapter.

The signals, AdrLo (15:0) (the 16 least-significant address lines), are sampled and pipelined by the 92A96 Module for two cycles. The signals are sampled one phase earlier than most of the signals because during cache accesses, the R3000 presents the low order address one phase early.

Tag (31:16), Data bus, MemRd* and MemWr* and all remaining control signals except AccTyp(2:0) and Run* are sampled and pipelined by the 92A96 for one cycle. The sample point occurs one clock cycle after AdrLo is sampled.

The AccTyp(2:0) and Run* signals are sampled with no pipeline delays. Although the other signals are sampled on every clock phase, these signals are sampled on Data Phases only. The sample point occurs one clock cycle after the single pipelined sample point when constructing an Instruction Phase. This provides access type and run/stall information on the Instruction and Data Phases. This information is therefore provided concurrent with the other phase information even though the signals are not guaranteed to be stable until the Data Phase.

The R3000 also provides a read mode known as block refill. The block refill quickly transfers a block of data into one of the caches. When block refills are enabled, one word per cycle is transferred into the cache after the RdBusy signal indicates that the access time has been satisfied. Figure B-1 does not include a block refill cycle. If block refills were present, there would be additional samples indicated just preceding the I3 samples.

Figure B-1 shows where signals are sampled for both cache and memory transfers. The memory transfer is shown as an Instruction transfer with one additional Stall cycle asserted via the RdBusy signal. The difference between an Instruction transfer and a Data transfer is that for a Data transfer, the data on the data bus is transferred during the Data Phase instead of the Instruction Phase.
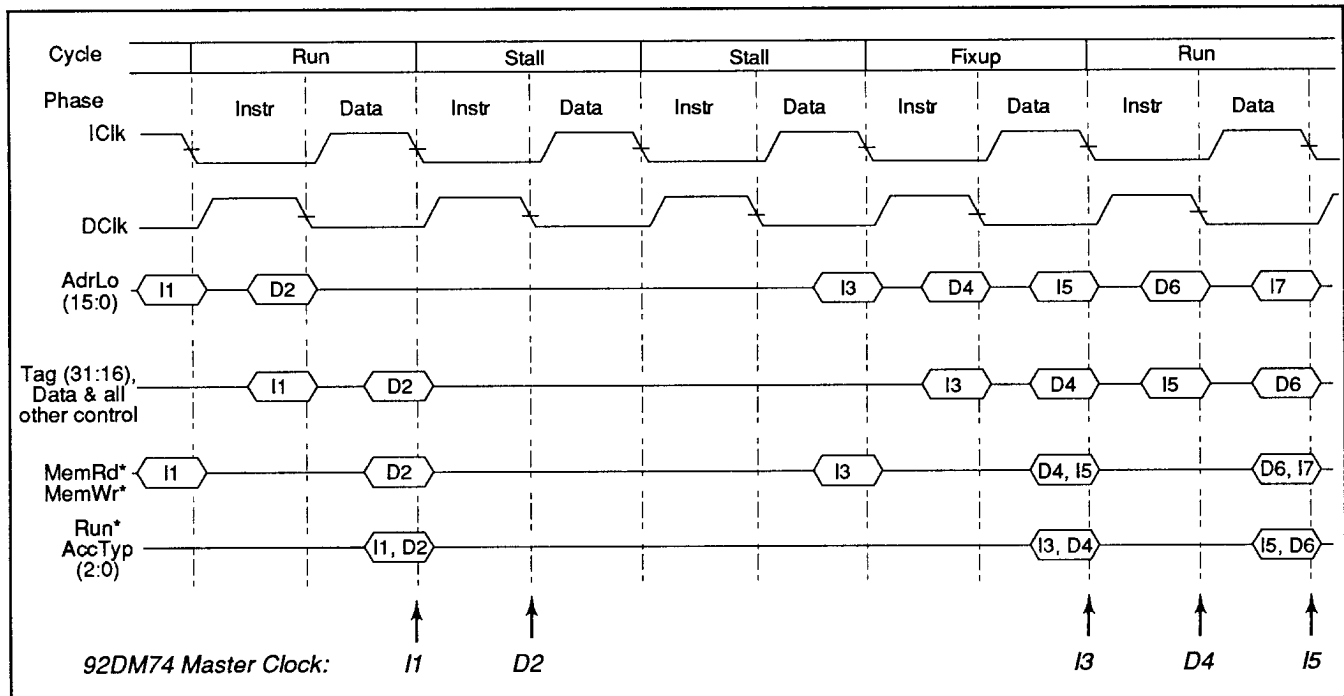
Figure B-1   Memory read, single-word instruction cache miss. The clocking choice for the Included Stall Phases is either Fixup and First Refill or Fixup and All Refills. The first Stall phase may or may not be acquired based on what causes the Stall phase.

CUSTOM CLOCKING

The Custom clocking algorithm offers six clocking variations selectable through two select fields in the Clock menu. The Included Stall Phases field has three selections: Fixup and First Refill (default selection), Fixup and All Refills, and All. The Run Cycle Data Phases field has two selections: Excludes Unused & CP Xfer (default selection) and Includes All.

The default selections filter out as many unimportant samples as possible to pack the maximum amount of CPU activity in the 92A96 Module's acquisition memory. You can use the other selections to acquire greater detail on Stall cycles and coprocessor transfers.

- **Included Stall Phases: Fixup and First Refill.** This selection filters out all stall phases except those required by the disassembler. Both phases of the Fixup cycle are needed because the clocking state machine cannot determine which phases contain valid data. The disassembler needs to know when a Refill phase occurs and whether it is an Instruction miss or Data miss so it can properly tag the cache miss phases. The Fixup and First Refill selection is the default selection.

- **Included Stall Phases: Fixup and All Refills.** This selection includes Fixup phases and all Refill phases.

- **Included Stall Phases: All.** This selection includes all Stall phases and is the least susceptible to timing violations on the clock qualifier channels. Refer to *Supplemental Timing Information* for more details on timing violations.

- **Run Cycle Data Phases: Excludes Unused & CP Xfer.** This selection filters out run-cycle data phases when no data is transferred. This phase usually does not contain useful information. However, the clocking state machine cannot differentiate a coprocessor transfer (that may have valid data on the bus) from an empty data phase. With this selection you can discard the coprocessor transfers and empty data phases without losing valuable information. The Coprocessor Transfers and Empty Data Phases Excluded is the default selection.

- **Run Cycle Data Phases: Includes All.** This selection includes all run cycle data phases.

ACQUIRED SIGNALS

The R3000 probe adapter connects to R3000 signals and enables the 92A96 Module to acquire them. See Table C-4 for a complete list of these signals and their channel assignments. The disassembler software then uses the signal information to disassemble the software program executing on your R3000 system. Not all acquired R3000 signals are needed by the disassembler software for disassembly.

The R3000 custom clocking uses all four clock channels and all four qualifiers. Clock 0 is the only stored clock signal (double probed with channel C0:7). Signals acquired by the four qualifier channels are latched by the circuitry on the probe adapter to guarantee that the 92A96 Module's setup and hold times are not violated. These signals are required by the disassembler as well as the 92A96 for Custom Clocking.

The Clock 0 and Clock 1 signals are synthesized signals. Clock 0 is the logical OR of the Data Cache read and write signals (DRd* and DWr*) and combines other signals that indicate whether the current cycle is a Fixup cycle. Clock 1 is the logical OR of the Instruction Cache read and write signals (IRd* and IWr*) and the IRW_CS* signal (a synthesized signal that indicates whether or not the caches are swapped).

The R3000 signals that the 92A96 Module acquires are described in IDT's *R3000 Hardware User Manuals*. Some of these signals are not required for disassembly. Table B-1 shows these signals. The disassembler provides these signals for you to view (when you change the default display radix from Off to the desired radix) or to use for hardware analysis. Refer to *Section 5: Hardware Analysis* for a description of Internal and External clocking choices.

Refer also to *Alternate Connections* to learn how to use these channels to make alternate R3000 system connections.

Table B-1
Signals Not Required for Disassembly

Signal	Use
Int*(5), Int*(4), Int*(4), Int*(2), Int*(1), Int*(0)	Intr group signals. The default radix is Off in the State menu.
CpSync*, BusError*, CpCond3 (AdrLo17), CpCond2 (AdrLo16), CpCond1, CpCond0, CpBusy, TagV, DRW_Fixup*	Misc group signals. The default radix is Off in the State menu.

SIGNALS NOT ACQUIRED

A single 92A96 Module does not have enough channels to acquire all the signals from the R3000 microprocessor. Table B-2 lists the channels not acquired by the 92A96 Module but are connected to the AUX connector on the probe adapter. You can use another DAS 9200 data acquisition module or move some of the podlets from the signals listed in Table B-1 to acquire and display these signals.

Table B-2
R3000 Signals Not Acquired

Signal	AUX Connector Location
CSwap†	11
DataP3	10
DataP2	9
DataP1	8
DataP0	7
Tag(15)	6
Tag(14)	5
Tag(13)	4
Tag(12)	3
TagP2	2
TagP1	1
TagP0	0
SysOut*‡	
† A synthesized signal; logic high when the caches are swapped and low when they are not. Use this signal in the Trigger menu to isolate transfers to swapped caches. ‡ Used by the probe adapter to synthesize the CSwap signal, connected to two pins of the 74F5074 but not to the AUX connector.	

The following signals are not acquired by the 92A96 Module and are not connected to the probe adapter:

ClK2xSys	Clk2xSmp	Clk2xRd	Clk2xPhi
DRd2*	DWr2*	IRd2*	IWr2*

If you want to acquire the above signals and the SysOut* signal, you must access them from other points on your system under test. Note that the CpSync* signal is acquired and is identical to the SysOut* signal.

SUPPLEMENTAL TIMING INFORMATION

The R3000 and R3000A family of devices are implementations of a MIPS Computer Systems Inc. (MIPS) design and is manufactured by several vendors. Among the different vendors, various speed versions are available. The 16 MHz, 20 MHz, and 25 MHz R3000 devices all conform to one set of timing specifications which are controlled by MIPS Computer Systems Inc. Versions that run at 33 MHz and faster have timing specifications that differ from vendor to vendor. Because of this, the 92DM74 disassembler software and 92A96 Module must satisfy a varying set of timing constraints and it may be necessary to analyze the 92DM74 timing requirements on a vendor-specific basis.

In some cases where the 92DM74 timing requirements do not meet all worst-case specifications, you may experience some of the disassembly problems listed under *Other Disassembly Problems* in Appendix A. To verify if the disassembly problems are caused by the R3000 or the SUT timing, look at the timing constraints that must be satisfied for the 92DM74 to acquire valid data. Use the timing constraints to assure that the results of the timing analysis for your R3000 system match the information in Tables B3–B6. To use the tables properly, you may need to have available the timing analysis for your R3000 system. The timing constraints are listed with each table and an example of how to use the timing constraints is provided at the end of this section.

Tables B3–B6 list the timing specifications required for the 16 MHz, 20 MHz, 25 MHz, and 33 MHz versions. The performance characteristics in the tables are valid under the following conditions:

- The probe adapter must be operating as an integral part of an appropriately configured R3000 instrument system.

- The instrument system must be in an operating environment whose limits are specified in Table C-3.

- The probe adapter must be properly connected to an R3000 SUT and must be provided with the proper power supply voltage described in Table C-1.

Some of the R3000 signals are more likely to violate the 92DM74 timing requirements than others. These signals include the Exc*, MemRd*, and MemWr* signals. Of these, the Exc* (Exception*) signal is the most likely signal to exhibit a timing violation. The following paragraphs describe some of the effects you might see for each of these signals:

- Exc*—this signal establishes the occurrence of a Fixup cycle. If Exc* is removed too early (the signal is too fast), the Fixup cycle is incorrectly interpreted as just another Stall cycle. This causes some cycles following the Fixup cycle not to be acquired. This condition can occur whenever the Clk2xPhi delay has been set to less than 6 ns. To minimize the impact of this timing violation, two of the clocking choices will continue to operate properly regardless of the timing of the Exc* signal. These choices are provided by selecting **Included Stall Phase: All** and either **Run Cycle Data Phases: Excludes Unused & CP Xfer** or **Run Cycle Data Phases: All**.

   If an Interrupt Grant is indicated and is immediately followed by a Coprocessor Busy Stall, or if a Coprocessor Busy Fixup is followed by a Stall, then the T_{SExc} specification is in effect and the Exc* signal can be incorrectly sampled as a logic low due to the signal being removed too late (the signal is too slow). Both of these conditions will cause a Stall cycle to be incorrectly interpreted as a Fixup cycle. This can cause extra samples to be acquired and indicated as phases of a Fixup cycle. However, this will not cause any problems for the disassembler since no cache or memory control strobes will be asserted.

- MemRd*—during the first stall of a memory read cycle, the T_{MRdI} timing can miss when the MemRd* signal is asserted. Since data is never transferred during the first Stall cycle, this should not cause any problems for the custom clocking or the disassembler. The only indication of this happening would be that the value of the MemRd* signal is incorrect when all Stall phases are acquired.

- MemWr*—the assertion and removal of the MemWr* signal can violate the 92DM74 Qualifier Setup requirement (acquisition of the signal, as opposed to clock qualification, requires 1.5 ns less setup time). If the assertion of the MemWr* signal is missed, the run cycle data phases with valid data writes can be discarded or mislabeled. If its removal is missed, run cycle data phases with no valid data transfers can inadvertently be acquired or the samples can be mislabeled.

In addition to timing violations causing the wrong value to be sampled, they can also cause metastable conditions. If a clock or qualifier signal causes a metastable condition, the acquired data stream can include extra erroneous data samples, incomplete data samples, or missing data samples.

In the following tables, the terms Maximum Margin and Minimum Margin are comparisons between the R3000 specifications and the 92DM74 requirements. A positive value indicates that the 92DM74 should work in all cases. However, a negative value indicates the 92DM74 may not work properly under all conditions; you may have to adjust your system timing or derate the R3000 or 92DM74 specifications. Refer to Example 2 at the end of this section for an example where the timing specifications must be derated.

Table B-3
AC Characteristics of a 16-MHz R3000 Running at 16.67 MHz

Parameter	92DM74 Requirements	R3000 Specification	Comments & Timing Constraints
Input Clock Timing			
Clock Period		30 ns to 1 μs	
Minimum	10.0 ns		
Minimum Margin	20 ns		
Clk2xSys to Clk2xSmp	No direct requirement	0 to 15 ns	
T_{sys} - T_{smp}			
Clk2xSmp to Clk2xRd		0 to 15 ns	Min > 0 ns if IClk and DClk timing is skewed by loading.
T_{smp} - T_{rd}			
Minimum	0 ns		
Minimum Margin	0 ns		
Maximum	$T_{cyc}/2$ - 11.5 ns		$(T_{smp} - T[rd]) \le (T_{cyc}/2) - 11.5$ ns
Maximum Margin	3.5 ns		
Clk2xSmp to Clk2xPhi		9 to 15 ns	$T_{smp} \ge -T_{Exc}(min) + T_{PAL\_pd}(max) + T_{373\_hld}$
T_{smp}			
Minimum	6.5 ns - $T_{Exc}(min)$		$T_{smp} \le T_{cyc}/2 - T_{SExc}(max) + T_{PAL\_pd}(min) - T_{373\_su}$
Minimum Margin	3.5 ns		
Maximum †	$T_{cyc}/2 - T_{SExc}(max) +$ 1.5 ns		$T_{smp} \le 11.5$ ns, or Exc* may not be properly latched
Maximum Margin	- 3.5 ns		
Maximum §	T_{cyc} - 14.2 ns - $T_{SExc}(max)$		
Maximum Margin	10.8 ns		
Clk2xSys to Clk2xRd		0 to 30 ns	
T_{sys}-T_{rd}			
Minimum	1.0 ns		$(T_{sys} - T_{rd}) \ge 1.0$ ns
Minimum Margin	-1.0 ns		
Maximum	$T_{cyc}/2$ - 7.0 ns		$(T_{sys} - T_{rd}) \le T_{cyc}/2 - 7.0$ ns
Maximum Margin	-7.0 ns		
Data Setup	5.0 ns	9.0 ns	
T_{DS} Margin	4.0 ns		
Data Hold	0.0 ns	-2.5 ns	
T_{DH} Margin	-2.5ns		Requires 0 ns Hold
CpBusy Setup	T_{smp} + 5.0 ns	13.0 ns	Will not affect disassembler if acquired incorrectly.
T_{CBS} Margin	8.0 ns - T_{smp}		
CpBusy Hold	-T_{smp}	-2.5 ns	Will not affect disassembler if acquired incorrectly.
T_{CBH} Margin	T_{smp} - 2.5 ns		
Write Delay		0 to 5 ns	
T_{WrDly} Minimum	-3.5 ns		
Minimum Margin	3.5 ns		
T_{WrDly} Maximum	$T_{cyc}/2$ - 11.5 ns		
Maximum Margin	13.5 ns		

(Cont.)

Table B-3 (Cont.)
AC Characteristics of a 16-MHz R3000 Running at 16.67 MHz

Parameter	92DM74 Requirements	R3000 Specification	Comments & Timing Constraints
AccTyp $(2{:}0)T_{SAcTy}$ $(1{:}0)T_{SAcTy}$ $(2)T_{SAcTy}$		0 to 27 ns	
Minimum	$-T_{smp}$		
Minimum Margin	T_{smp}		
Maximum	$T_{cyc} - T_{smp} - 5ns$		
Maximum Margin	28 ns $- T_{smp}$		
Memory Read Initiate T_{MRdI}		1 to 27 ns	
Terminate T_{MRdT}		1 to 7 ns	
Both: Minimum	$-T_{smp} + 2$ ns		
Minimum Margin	$T_{smp} - 1$ ns		
Maximum	$T_{cyc} - T_{smp} - 11.5$ ns		$T_{MRdI}(max) \le T_{cyc} - T_{smp} - T_{PAL\_pd}(max) - T_{A96\_qual\_su}$
Maximum Margin	21.5 ns $- T_{smp}$		
Memory Write T_{MWr}, T_{SMWr}		1 to 27 ns	
Minimum	$-T_{smp} + 2$ ns		
Minimum Margin	$T_{smp} - 1$ ns		
Maximum	$T_{cyc} - T_{smp} - 11.5$ ns		$T_{MRdI}(max) \le T_{cyc} - T_{smp} - T_{PAL\_pd}(max) - T_{A96\_qual\_su}$
Maximum Margin	21.5 ns $- T_{smp}$		
Exception T_{Exc}		0 to 7 ns	(Also see T_{smp} specification)
Minimum †	$-T_{smp} + 6.5$ ns		$T_{smp}(min) = 9$ ns; therefore Minimum Margin = 2.5 ns
Minimum Margin	$T_{smp} - 6.5ns$		
Maximum ‡	$T_{cyc}/2 - T_{smp} - 5$ ns		$T_{smp}(max) = 15$ ns; therefore
Maximum Margin	18 ns $- T_{smp}$		Maximum Margin = 3.0 ns
Exception T_{SExc}		3 to 20 ns	(Also see T_{smp} specification)
Minimum †	$-T_{smp} + 6.5$ ns		$T_{smp}(min) = 9$ ns; therefore Minimum Margin = 5.5 ns
Minimum Margin	$T_{smp} - 3.5ns$		
Maximum‡	$T_{cyc}/2 - T_{smp} - 5$ ns		$T_{SExc}(max) \le T_{cyc}/2 - T_{smp} - T_{A96\_su}$
Maximum Margin	5 ns $- T_{smp}$		$T_{smp}(max) = 15$ ns; therefore Maximum Margin = -10 ns Propagation delay of Exc* must be significantly less than worst-case, or invalid data will be acquired
T_{SExc} Maximum †	$T_{cyc}/2 - T_{smp} + 1.5$ ns		$T_{smp}(max) = 15$ ns; therefore Maximum Margin = -3.5 ns
Maximum Margin	11.5 ns $- T_{smp}$		T_{smp} should be less than or equal to 11.5 ns

Table B-3 (Cont.)
AC Characteristics of a 16-MHz R3000 Running at 16.67 MHz

Parameter	92DM74 Requirements	R3000 Specification	Comments & Timing Constraints
Address Valid T_{SAVal} Minimum Minimum Margin Maximum Maximum Margin	$-T_{smp}$ T_{smp} $T_{cyc} - T_{smp} - 5$ ns 25 ns $- T_{smp}$	0 to 30 ns	
Run Terminate T_{Stl}		3 to 17 ns	
Run Initiate T_{Run} Both Minimum Minimum Margin Maximum Maximum Margin	$-T_{smp} + 2$ ns $T_{smp} - 1.0$ ns $T_{cyc} - T_{smp} - 11.5$ ns 31.5 ns $- T_{smp}$	1 to 7 ns	
† Due to 74FCT373CT latch ‡ Due to 92A96 Module acquisition of Exc* signal § Due to 92A96 Module acquisition of DRW_Fixup* signal			

Table B-4
AC Characteristics of a 20-MHz R3000 Running at 20 MHz

Parameter	92DM74 Requirements	R3000 Specification	Comments & Timing Constraints

Input Clock Timing
Clock Period
  Minimum
  Minimum Margin
	
	10.0 ns
	15 ns
		25 ns to 1 μs	

Clk2xSys to Clk2xSmp $T_{sys} - T_{smp}$	No direct requirement	0 to 12.5 ns	

Clk2xSmp to Clk2xRd
$T_{smp} - T_{rd}$
  Minimum
  Minimum Margin
  Maximum
  Maximum Margin
	
	0 ns
	0 ns
	$T_{cyc}/2$ - 11.5 ns
	1.0 ns
		0 to 12.5 ns	Min > 0 ns if IClk and DClk timing is skewed by loading.
			
			$(T_{smp} - T_{rd}) \le (T_{cyc}/2)$ - 11.5 ns

Clk2xSmp to Clk2xPhi
T_{smp}
  Minimum
 	
  Minimum Margin
  Maximum †
 	
  Maximum Margin
  Maximum §
 	
  Maximum Margin
	
	6.5 ns - $T_{Exc}(min)$
	
	0.5 ns
	$T_{cyc}/2$ - $T_{SExc}(max)$ + 1.5 ns
	- 4.0 ns
	T_{cyc} - 14.2 ns - $T_{SExc}(max)$
	5.3 ns
		7 to 12.5 ns	$T_{smp} \ge -T_{Exc}(min) + T_{PAL\_pd}(max) + T_{373\_hld}$
			$T_{smp} \le T_{cyc}/2 - T_{SExc}(max) + T_{PAL\_pd}(min) - T_{373\_su}$
			
			$T_{smp} \le$ 8.5 ns, or Exc* may not be properly latched

Clk2xSys to Clk2xRd
$T_{sys} - T_{rd}$
  Minimum
  Minimum Margin
  Maximum
  Maximum Margin
	
	1.0 ns
	-1.0 ns
	$T_{cyc}/2$ - 7.0 ns
	-7.0 ns
		0 to 25 ns	
			
			$(T_{sys} - T_{rd}) \ge$ 1.0 ns
			
			$(T_{sys} - T_{rd}) \le T_{cyc}/2$ - 7.0 ns

Data Setup T_{DS} Margin	5.0 ns 3.0 ns	8.0 ns	
Data Hold T_{DH} Margin	0.0 ns -2.5ns	-2.5 ns	 Requires 0 ns Hold
CpBusy Setup T_{CBS} Margin	T_{smp} + 5.0 ns 6.0 ns - T_{smp}	11.0 ns	Will not affect disassembler if acquired incorrectly.
CpBusy Hold T_{CBH} Margin	-T_{smp} T_{smp} - 2.5 ns	-2.5 ns	Will not affect disassembler if acquired incorrectly.

Write Delay
T_{WrDly} Minimum
  Minimum Margin
T_{WrDly} Maximum
  Maximum Margin
	
	-3.5 ns
	3.5 ns
	$T_{cyc}/2$ - 11.5 ns
	9.5 ns
		0 to 4 ns	

(Cont.)

Table B-4 (Cont.)
AC Characteristics of a 20-MHz R3000 Running at 20 MHz

Parameter	92DM74 Requirements	R3000 Specification	Comments & Timing Constraints
AccTyp $(2{:}0)T_{SAcTy}$ $(1{:}0)T_{SAcTy}$ $(2)T_{SAcTy}$ Minimum Minimum Margin Maximum Maximum Margin	$-T_{smp}$ T_{smp} $T_{cyc} - T_{smp}$ - 5ns 22 ns - T_{smp}	0 to 23 ns	
Memory Read Initiate T_{MRdI} Terminate T_{MRdT} Both: Minimum Minimum Margin Maximum Maximum Margin	$-T_{smp}$ + 2 ns T_{smp} - 1 ns $T_{cyc} - T_{smp}$ -11.5 ns 15.5 ns - T_{smp}	1 to 23 ns 1 to 7 ns	$T_{MRdI}(max) \leq T_{cyc} - T_{smp} -$ $T_{PAL\_pd}(max) - T_{A96\_qual\_su}$
Memory Write T_{MWr}, T_{SMWr} Minimum Minimum Margin Maximum Maximum Margin	$-T_{smp}$ + 2 ns T_{smp} - 1 ns $T_{cyc} - T_{smp}$ - 11.5 ns 15.5 ns - T_{smp}	1 to 23 ns	$T_{MRdI}(max) \leq T_{cyc} - T_{smp} -$ $T_{PAL\_pd}(max) - T_{A96\_qual\_su}$
Exception T_{Exc} Minimum † Minimum Margin Maximum ‡ Maximum Margin	$-T_{smp}$ + 6.5 ns T_{smp} - 6.5 ns $T_{cyc}/2 - T_{smp}$ - 5 ns 14 ns - T_{smp}	0 to 6 ns	(Also see T_{smp} specification) $T_{smp}(min)$ = 7 ns; therefore Minimum Margin = 0.5 ns $T_{smp}(max)$ = 12.5 ns; therefore Maximum Margin = 1.5 ns
Exception T_{SExc} Minimum † Minimum Margin Maximum ‡ Maximum Margin	$-T_{smp}$ + 6.5 ns T_{smp} - 3.5ns $T_{cyc}/2 - T_{smp}$ - 5 ns 2.0 ns - T_{smp}	3 to 18 ns	(Also see T_{smp} specification) $T_{smp}(min)$ = 7 ns; therefore Minimum Margin = 3.5 ns $T_{SExc}(max) \leq T_{cyc}/2 - T_{smp} -$ T_{A96_su} $T_{smp}(max)$ = 12.5 ns; therefore Maximum Margin = -10.5 ns Propagation delay of Exc* must be significantly less than worst-case, or invalid data will be acquired
T_{SExc} Maximum † Maximum Margin	$T_{cyc}/2 - T_{smp}$ + 1.5 ns 8.5 ns - T_{smp}		$T_{smp}(max)$ = 12.5 ns; therefore Maximum Margin = -4.0 ns T_{smp} should be less than or equal to 8.5 ns

(Cont.)

Table B-4 (Cont.)
AC Characteristics of a 20-MHz R3000 Running at 20 MHz

Parameter	92DM74 Requirements	R3000 Specification	Comments & Timing Constraints
Address Valid T_{SAVal}		0 to 25 ns	
Minimum	$-T_{smp}$		
Minimum Margin	T_{smp}		
Maximum	$T_{cyc} - T_{smp} - 5$ ns		
Maximum Margin	20 ns $- T_{smp}$		
Run Terminate T_{Stl}		3 to 15 ns	
Run Initiate T_{Run}		1 ns to 6 ns	
Both			
Minimum	$-T_{smp} + 2$ ns		
Minimum Margin	$T_{smp} - 1.0$ ns		
Maximum	$T_{cyc} - T_{smp} - 11.5$ ns		
Maximum Margin	23.5 ns $- T_{smp}$		

† Due to 74FCT373CT latch
‡ Due to 92A96 Module acquisition of Exc* signal
§ Due to 92A96 Module acquisition of DRW_Fixup* signal

Table B-5
AC Characteristics of a 25-MHz R3000 Running at 25 MHz

Parameter	92DM74 Requirements	R3000 Specification	Comments & Timing Constraints
Input Clock Timing Clock Period Minimum Minimum Margin	10.0 ns 10 ns	20 ns to 1 μs	
Clk2xSys to Clk2xSmp $T_{sys} - T_{smp}$	No direct requirement	0 to 10 ns	
Clk2xSmp to Clk2xRd $T_{smp} - T_{rd}$ Minimum Minimum Margin Maximum Maximum Margin	0 ns 0 ns $T_{cyc}/2 - 11.5$ ns -1.5 ns	0 to 10 ns	Min > 0 ns if IClk and DClk timing is skewed by loading. $(T_{smp} - T_{rd}) \leq (T_{cyc}/2) - 11.5$ ns
Clk2xSmp to Clk2xPhi T_{smp} Minimum Minimum Margin Maximum † Maximum Margin Maximum § Maximum Margin	6.5 ns - T_{Exc}(min) -1.5 ns $T_{cyc}/2 - T_{SExc}$(max) + 1.5 ns - 3.5 ns $T_{cyc} - 14.2$ ns - T_{SExc}(max) 0.8 ns	5 to 10 ns	$T_{smp} \geq -T_{Exc}$(min) + T_{PAL_pd}(max) + T_{373_hld} $T_{smp} \leq T_{cyc}/2 - T_{SExc}$(max) + T_{PAL_pd}(min) - T_{373_su} $T_{smp} \leq 6.5$ ns, or Exc* may not be properly latched
Clk2xSys to Clk2xRd $T_{sys} - T_{rd}$ Minimum Minimum Margin Maximum Maximum Margin	1.0 ns -1.0 ns $T_{cyc}/2 - 7.0$ ns -7.0 ns	0 to 20 ns	$(T_{sys} - T_{rd}) \geq 1.0$ ns $(T_{sys} - T_{rd}) \leq T_{cyc}/2 - 7.0$ ns
Data Setup T_{DS} Margin	5.0 ns 1.0 ns	6.0 ns	
Data Hold T_{DH} Margin	0.0 ns -2.5ns	-2.5 ns	Requires 0 ns Hold
CpBusy Setup T_{CBS} Margin	T_{smp} + 5.0 ns 4.0 ns - T_{smp}	9.0 ns	Will not affect disassembler if acquired incorrectly.
CpBusy Hold T_{CBH} Margin	-T_{smp} T_{smp} - 2.5 ns	-2.5 ns	Will not affect disassembler if acquired incorrectly.
Write Delay T_{WrDly} Minimum Minimum Margin T_{WrDly} Maximum Maximum Margin	-3.5 ns 3.5 ns $T_{cyc}/2 - 11.5$ ns 5.5 ns	0 to 3 ns	

(Cont.)

92DM74 R3000/A Instructions

Table B-5 (Cont.)
AC Characteristics of a 25-MHz R3000 Running at 25 MHz

Parameter	92DM74 Requirements	R3000 Specification	Comments & Timing Constraints
AccTyp $(2:0)T_{SAcTy}$ $(1:0)T_{SAcTy}$ $(2)T_{SAcTy}$		0 to 18 ns	
Minimum	$-T_{smp}$		
Minimum Margin	T_{smp}		
Maximum	$T_{cyc} - T_{smp} - 5ns$		
Maximum Margin	$17\text{ ns} - T_{smp}$		
Memory Read Initiate T_{MRdI}		0 to 18 ns	
Terminate T_{MRdT}		0 to 5 ns	
Both: Minimum	$-T_{smp} + 2$ ns		
Minimum Margin	$T_{smp} - 2$ ns		
Maximum	$T_{cyc} - T_{smp} -11.5$ ns		$T_{MRdI}(max) \leq T_{cyc} - T_{smp} - T_{PAL\_pd}(max) - T_{A96\_qual\_su}$
Maximum Margin	$10.5\text{ ns} - T_{smp}$		
Memory Write T_{MWr}, T_{SMWr}		0 to 18 ns	
Minimum	$-T_{smp} + 2$ ns		
Minimum Margin	$T_{smp} - 2$ ns		
Maximum	$T_{cyc} - T_{smp} - 11.5$ ns		$T_{MRdI}(max) \leq T_{cyc} - T_{smp} - T_{PAL\_pd}(max) - T_{A96\_qual\_su}$
Maximum Margin	$10.5\text{ ns} - T_{smp}$		
Exception T_{Exc}		0 to 5 ns	(Also see T_{smp} specification) $T_{smp}(min) = 5$ ns; therefore
Minimum †	$-T_{smp} + 6.5$ ns		Minimum Margin = -1.5 ns
Minimum Margin	$T_{smp} - 6.5$ ns		$T_{smp}(max) = 10$ ns; therefore
Maximum ‡	$T_{cyc}/2 - T_{smp} - 5$ ns		Maximum Margin = 0 ns
Maximum Margin	$10\text{ ns} - T_{smp}$		
Exception T_{SExc}		3 to 15 ns	(Also see T_{smp} specification) $T_{smp}(min) = 5$ ns; therefore
Minimum †	$-T_{smp} + 6.5$ ns		Minimum Margin = 1.5 ns
Minimum Margin	$T_{smp} - 3.5ns$		$T_{SExc}(max) \leq T_{cyc}/2 - T_{smp} - T_{A96\_su}$
Maximum ‡	$T_{cyc}/2 - T_{smp} - 5$ ns		$T_{smp}(max) = 10$ ns; therefore
Maximum Margin	$-T_{smp}$		Maximum Margin = -10 ns Propagation delay of Exc* must be significantly less than worst-case, or invalid data will be acquired
T_{SExc} Maximum †	$T_{cyc}/2 - T_{smp} + 1.5$ ns		$T_{smp}(max) = 10$ ns; therefore
Maximum Margin	$6.5\text{ ns} - T_{smp}$		Maximum Margin = -3.5 ns T_{smp} should be less than or equal to 6.5 ns

(Cont.)

Table B-5 (Cont.)
AC Characteristics of a 25-MHz R3000 Running at 25 MHz

Parameter	92DM74 Requirements	R3000 Specification	Comments & Timing Constraints
Address Valid T_{SAVal} Minimum Minimum Margin Maximum Maximum Margin	$-T_{smp}$ T_{smp} $T_{cyc} - T_{smp} - 5$ ns 15 ns $- T_{smp}$	0 to 20 ns	
Run Terminate T_{Stl}		3 to 11 ns	
Run Initiate T_{Run} Both Minimum Minimum Margin Maximum Maximum Margin	$-T_{smp} + 2$ ns $T_{smp} - 1.0$ ns $T_{cyc} - T_{smp} - 11.5$ ns 17.5 ns $- T_{smp}$	1 to 4 ns	

† Due to 74FCT373CT latch
‡ Due to 92A96 Module acquisition of Exc* signal
§ Due to 92A96 Module acquisition of DRW_Fixup* signal

     92DM74 R3000/A Instructions

Table B-6
AC Characteristics of a 33-MHz R3000A Running at 33.33 MHz

Parameter	92DM74 Requirements	R3000 Specification	Comments & Timing Constraints
Input Clock Timing Clock Period		15 ns to 1 μs	
Minimum	10.0 ns		
Minimum Margin	5 ns		
Clk2xSys to Clk2xSmp $T_{sys} - T_{smp}$	No direct requirement	0 to 7.5 ns	
Clk2xSmp to Clk2xRd $T_{smp} - T_{rd}$		0 to 7.5 ns	Min > 0 ns if IClk and DClk timing is skewed by loading.
Minimum	0 ns		
Minimum Margin	0 ns		
Maximum	$T_{cyc}/2 - 11.5$ ns		$(T_{smp} - T_{rd}) \leq (T_{cyc}/2) - 11.5$ ns
Maximum Margin	-4.0 ns		
Clk2xSmp to Clk2xPhi T_{smp}		4 to 7.5 ns	$T_{smp} \geq -T_{Exc}(min) + T_{PAL\_pd}(max) + T_{373\_hld}$
Minimum	6.5 ns - $T_{Exc}(min)$		$T_{smp} \leq T_{cyc}/2 - T_{SExc}(max) + T_{PAL\_pd}(min) - T_{373\_su}$
Minimum Margin	-2.5 ns		
Maximum †	$T_{cyc}/2 - T_{SExc}(max) +$ 1.5 ns		$T_{smp} \leq 6.5$ ns, or Exc* may not be properly latched
Maximum Margin	- 1.0 ns		
Maximum §	$T_{cyc} - 14.2$ ns - $T_{SExc}(max)$		TSExc(max) varies between vendors, compensate if appropriate
Maximum Margin	-1.7 ns		
Clk2xSys to Clk2xRd $T_{sys} - T_{rd}$		0 to 15 ns	
Minimum	1.0 ns		$(T_{sys} - T_{rd}) \geq 1.0$ ns
Minimum Margin	-1.0 ns		
Maximum	$T_{cyc}/2 - 7.0$ ns		$(T_{sys} - T_{rd}) \leq T_{cyc}/2 - T_{PAL\_pd}(max) - 2$ ns
Maximum Margin	-7.0 ns		
Data Setup T_{DS} Margin	5.0 ns 0 ns	5.0 ns	
Data Hold T_{DH} Margin	0.0 ns -2.5ns	-2.5 ns	Requires 0 ns Hold
CpBusy Setup T_{CBS} Margin	$T_{smp} + 5.0$ ns 2.0 ns - T_{smp}	7.0 ns	Will not affect disassembler if acquired incorrectly.
CpBusy Hold T_{CBH} Margin	$-T_{smp}$ $T_{smp} - 2.5$ ns	-2.5 ns	Will not affect disassembler if acquired incorrectly.
Write Delay		0 to 2.0 ns	
T_{WrDly} Minimum	-3.5 ns		
Minimum Margin	3.5 ns		
T_{WrDly} Maximum	$T_{cyc}/2 - 11.5$ ns		
Maximum Margin	1.5 ns		

(Cont.)

Table B-6 (Cont.)
AC Characteristics of a 33-MHz R3000A Running at 33.33 MHz

Parameter	92DM74 Requirements	R3000 Specification	Comments & Timing Constraints
AccTyp $(2:0)T_{SAcTy}$ $(1:0)T_{SAcTy}$ $(2)T_{SAcTy}$ Minimum Minimum Margin Maximum Maximum Margin	$-T_{smp}$ T_{smp} $T_{cyc} - T_{smp} - 5ns$ $11.5\ ns - T_{smp}$	0 to 13.5 ns	
Memory Read Initiate T_{MRdI} Terminate T_{MRdT} Both: Minimum Minimum Margin Maximum Maximum Margin	$-T_{smp} + 2\ ns$ $T_{smp} - 2\ ns$ $T_{cyc} - T_{smp} - 11.5\ ns$ $5.0\ ns - T_{smp}$	0 to 13.5 ns 0 to 3.5 ns	$T_{MRdI}(max) \leq T_{cyc} - T_{smp} -$ $T_{PAL\_pd}(max) - T_{A96\_qual\_su}$ Tsmp $\geq$ 5 ns requires derate
Memory Write $T_{MWr},\ T_{SMWr}$ Minimum Minimum Margin Maximum Maximum Margin	$-T_{smp} + 2\ ns$ $T_{smp} - 2\ ns$ $T_{cyc} - T_{smp} - 11.5\ ns$ $5.0\ ns - T_{smp}$	0 to 13.5 ns	$T_{MRdI}(max) \leq T_{cyc} - T_{smp} -$ $T_{PAL\_pd}(max) - T_{A96\_qual\_su}$ $T_{smp} \geq$ 5 ns requires derate (Also see T_{smp} specification)
Exception T_{Exc} Minimum † Minimum Margin Maximum ‡ Maximum Margin	$-T_{smp} + 6.5\ ns$ $T_{smp} - 6.5\ ns$ $T_{cyc}/2 - T_{smp} - 5\ ns$ $6.5\ ns - T_{smp}$	0 to 3.5 ns	$T_{smp}(min) = 4$ ns; therefore Minimum Margin = -2.5 ns Okay if $T_{smp} = 6.5$ ns $T_{smp}(max) = 7.5$ ns; therefore Maximum Margin = -1.0 ns (Also see T_{smp} specification)
Exception T_{SExc} Minimum † Minimum Margin Maximum ‡ Maximum Margin	$-T_{smp} + 6.5\ ns$ $T_{smp} - 4.5ns$ $T_{cyc}/2 - T_{smp} - 5\ ns$ $-T_{smp}$	2 to 10 ns	$T_{smp}(min) = 4$ ns; therefore Minimum Margin = -0.5 ns $T_{SExc}(max) \leq T_{cyc}/2 - T_{smp} -$ T_{A96_su} $T_{smp}(max) = 7.5$ ns; therefore Maximum Margin = -7.5 ns Propagation delay of Exc* must be significantly less than worst-case, or invalid data will be acquired
T_{SExc} Maximum † Maximum Margin	$T_{cyc}/2 - T_{smp} + 1.5\ ns$ $6.5\ ns - T_{smp}$		$T_{smp}(max) = 7.5$ ns; therefore Maximum Margin = -1.0 ns T_{smp} should be less than or equal to 6.5 ns

(Cont.)

Table B-6 (Cont.)
AC Characteristics of a 33-MHz R3000A Running at 33.33 MHz

Parameter	92DM74 Requirements	R3000 Specification	Comments & Timing Constraints
Address Valid T_{SAVal}		0 to 15 ns	
Minimum	$-T_{smp}$		
Minimum Margin	T_{smp}		
Maximum	$T_{cyc} - T_{smp} - 5$ ns		
Maximum Margin	10 ns $- T_{smp}$		
Run Terminate T_{Stl}		0 to 8 ns	
Run Initiate T_{Run}		0 to 3 ns	
Both			
Minimum	$-T_{smp} + 2$ ns		
Minimum Margin	$T_{smp} - 2.0$ ns		
Maximum	$T_{cyc} - T_{smp} - 11.5$ ns		
Maximum Margin	10.5 ns $- T_{smp}$		
† Due to 74FCT373CT latch			
‡ Due to 92A96 Module acquisition of Exc* signal			
§ Due to 92A96 Module acquisition of DRW_Fixup* signal			

The following paragraphs provide examples of using the timing constraints for an R3000 SUT at 33 MHz.

Example 1. To generate and acquire the Fixup portion of the synthesized DRW_Fixup* signal can require two calculations. The first calculation is to properly latch the Fixup indication into the 74FCT373CT. Use the following expression:

$$T_{smp}(max) \leq T_{cyc}/2 - T_{SExc}(max) + T_{PAL\_pd}(min) - T_{373\_su}$$

Yields (at 33 MHz, worst-case slow R3000A, worst-case fast PAL, and latch setup time:

$$T_{smp}(max) \leq 15 \text{ ns} - 10 \text{ ns} + 3.5 \text{ ns} - 2.0 \text{ ns}$$
$$\leq 6.5 \text{ ns} @ 33 \text{ MHz}$$

The second calculation is to acquire the Fixup indication on the DRW_Fixup* signal:

$$T_{373\_pd} + T_{PAL\_pd} \leq T_{cyc}/2 - T_{PAL\_pd}(min) + T_{373\_su} - T_{A96\_su}$$
$$\leq 15 \text{ ns} - 3.5 \text{ ns} + 2.0 \text{ ns} - 5.0 \text{ ns}$$
$$\leq 8.5 \text{ ns}$$

However:

$$T_{373\_pd} + T_{PAL\_pd} = 4.2 \text{ ns} + 5 \text{ ns} = 9.2 \text{ ns}$$

The 9.2 ns is not less than 8.5 ns and misses by 0.7 ns. Therefore, you must derate the value by 0.7 ns. This is reasonable since it involves the maximum propagation delay of one PAL and the 74FCT373CT, and the setup time of the 92A96 Module. It also presumes T_{SExc} is at maximum. The minimum propagation delay of the second PAL and the latch setup time defines the point at which the Exc* signal can switch and still be validly sampled by the latch.

Example 2. Calculate the value of the Exc* signal when directly acquired by the 92A96 Module.

$$T_{SExc}(max) \leq T_{cyc}/2 - T_{smp} - T_{A96\_su}$$

Yields (at 33 MHz, worst-case slow R3000A, and 92A96 Module setup time):

$$10 \text{ ns} \leq 15 \text{ ns} - T_{smp} - 5 \text{ ns}$$
$$T_{smp} \leq 0 \text{ ns}$$

This is not possible since T_{smp} is 4 ns minimum for a 33 MHz R3000A. Therefore, if the Exc* signal is to be correctly acquired for the cycles where the T_{SExc} specification is defining the timing, the T_{SExc} specification must be derated. Since this is a large violation, it is likely that the Exc* signal will not be acquired correctly. The symptoms of an incorrect acquisition would be that the disassembler incorrectly marks a sample as a Fixup cycle when it was a Stall cycle; however, the it should not cause a mnemonic disassembly error.

Example 3. Calculate MemRd* assertion (also MemWr* specifications T_{MWr} and T_{SMWr}):

$$T_{MRdI}(max) \leq T_{cyc} - T_{smp} - T_{PAL\_pd}(max) - T_{A96\_qual\_su}$$

Yields (at 33 MHz, worst-case slow R3000A, PAL and 92A96 Module setup time):

```
13.5 ns ≤ 30 ns - Tsmp - 5.0 ns - 6.5 ns
  Tsmp    ≤ 5.0 ns
```

This can be reasonably derated to $T_{smp} \leq 6.5$ ns since it involves worst-case slow R3000A, PAL, and the 92A96 setup time. None of these should be at worst-case simultaneously.

Warning

The following servicing instructions are for use only by qualified personnel. To avoid personnel injury, do not perform any servicing other than that contained in the operating instructions unless you are qualified to do so. Refer to General Safety Summary and Service Safety Summary prior to performing any service.

Appendix C:
SERVICE INFORMATION

This appendix contains the following information:

- safety summary

- brief description of the probe adapter and how it works

- care and maintenance

- specification tables

- channel assignment table

- dimensions of the standard and optional probe adapter with all four clock probes and twelve 8-channel probes connected

- removing and replacing individual podlets

- removing and replacing sockets

- replaceable electrical parts list

- circuit board component location diagrams

- schematics

- replaceable mechanical parts list

- exploded mechanical diagram

SERVICING SAFETY INFORMATION

The following service safety information is for service technicians. Follow these safety precautions, along with the general precautions outlined in your DAS 9200 acquisition module user's manual, while installing or servicing this product.

Do Not Service Alone. Do not perform internal service or adjustment on this product unless another person is present and able to give first aid and resuscitation.

Use Care When Servicing With Power On. To avoid personal injury from dangerous voltages, remove jewelry such as rings, watches, and other metallic objects before servicing. Do not touch the product's exposed connections and components while power is on.

PROBE ADAPTER DESCRIPTION

The probe adapter is a non-intrusive piece of hardware that allows the DAS 9200 to acquire data from an R3000/A microprocessor in its own operating environment with little effect, if any, on that system. The probe adapter consists of a circuit board with a ZIF socket for the R3000/A microprocessor and a small amount of active circuitry. It connects to four clock probes and twelve 8-channel probes.

Most signals from the R3000/A system flow from the probe adapter to square pins connected to the 92A96 clock and 8-channel probes. The signals then go across the 92A96 probe cables to the 92A96 Data Acquisition Module. Some of the signals not acquired by the 92A96 are connected to square pins on the probe adapter; these signals and the square pin connections are listed in Appendix B.

All circuitry on the probe adapter is powered from the system under test. Refer to *92A96 Custom Clocking* in Appendix B for a description of how the signals are acquired by 92A96 via the probe adapter. In addition to the active components on the probe adapter are two jumpers (Big/Little Endian and Timing/Normal). These jumpers must be placed in the correct position before acquiring data. Refer to *Configuring the Probe Adapter* in Sections 2 or 3 for more information on the jumper positions.

The probe adapter accommodates both the R3000 and R3000A microprocessors. The R3000A is available in either a 145-pin or 175-pin PGA package while the R3000 uses a 145-pin PGA package. The main difference between the two packages is that the 175-pin package has an extra inside row of pins that connect either to Vcc or ground. The three outside rows of pins of both packages are pin-compatible. The target board is designed to be compatible with both packages. The probe adapter replaces the microprocessor in the SUT and the microprocessor is then placed back in the ZIF socket on the top of the probe adapter.

CARE AND MAINTENANCE

The probe adapter does not require scheduled or periodic maintenance. To maintain good electrical contact, keep the probe adapter free of dirt, dust and contaminants. Also, ensure that any electrically conductive contaminants are removed.

Dirt and dust can usually be removed with a soft brush. For more extensive cleaning, use only a damp cloth. Abrasive cleaners and organic solvents should never be used.

```
┌─────────────────┐
│    CAUTION      │
└─────────────────┘
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The semiconductor devices contained on the probe adapter are susceptible to static-discharge damage. To prevent damage, service the probe adapter only in a static-free environment.

Always wear a grounding wrist strap, or similar device, while servicing the instrument.

Discharge stored static electricity from the probe adapter by, touching any of the ground pins (row of square pins closest to the edge of the probe adapter circuit board).

Exercise care when soldering on a multilayer circuit board. Excessive heat can damage the through-hole plating or lift a run or pad and damage the board beyond repair. Do not apply heat for longer than three seconds. Do not apply heat consecutively to adjacent leads. Allow a moment for the board to cool between each operation.

If you must replace an electrical component on a circuit board, exercise extreme caution while desoldering or soldering the new component. Use a pencil-type soldering iron of less than 18 watts and an approved desoldering tool. Use the proper soldering and desoldering techniques removing and replacing surface mounted components. Ensure that the replacement is an equivalent part by comparing the description as listed in the replaceable parts list.

SPECIFICATIONS

These specifications are for a probe adapter connected to a 92A96 Data Acquisition Module and the SUT. Table C-1 shows the electrical requirements the system under test must produce for the disassembler to acquire correct data. Table C-2 shows the physical specifications for the microprocessor support package and its associated options. Table C-3 shows the environmental specifications.

Table C-1
Electrical Specifications

Characteristics	Requirements
SUT DC Power Requirement	
Voltage	+5 V ±0.25 V
Current	400 mA max.
	300 mA typical
SUT Clock	
Clock Rate	33.3 MHz max.
(Falling Edge of IClk ORed with Falling Edge of DClk)	66.7 MHz max.
Time Between Falling Edge of IClk ORed with Falling Edge of DClk	15 ns min.
Minimum Setup Time (relative to falling edge of IClk ORed with falling edge of DClk)	
IRd*, Drd*, IWr*, Dwr*	10 ns †
IClk, DClk	10 ns †, ‡
MemRd*, MemWr*, Run*	11.5 ns †, §
Xen*	11.5 ns †
Exc*	5 ns ¶
All other signals	5 ns
Minimum Hold Time (relative to falling edge of IClk ORed with falling edge of DClk)	
IWr*, DWr*	-3 ns
MemRd*, MemWr*, Run*	-3 ns
IClk, DClk	0 ns
Exc*	6.5 ns #
All other signals	0 ns ††
Minimum Pulse Width (relative to falling edge of IClk ORed with falling edge of DClk)	
IRd*, DRd*, XEn*	7 ns

(Cont.)

Table C-1 (Cont.)
Electrical Specifications

Characteristics	Supplemental Information	
Maximum SUT Signal Loading	AC Load ‡‡	DC Load §§
AdrLo(15:0), Tag(31:16)	<20 pF	100 kΩ
Data	<20 pF	100 kΩ
Control		
IClk, DClk	<30 pF	100 kΩ + (1) 74F5074 + (2) 16L8-5
SysOut*	<20 pF	(2) 74F5074
Exc*	<25 pF	100 kΩ + (1) 74FCT
CpSync*	<20 pF	100 kΩ
IRd1*, IWr1*, DRd1*, DWr1*, XEn*	<15 pF	(1) 16L8-5
MemRd*, MemWr*, Run*		
All other Control	<20 pF	100 kΩ

† IRd1*, DRd1*, IWr1*, DWr1*, MemRd*, MemWr*, Run*, and XEn* signals are delayed by 3 to 5 ns when Normal/Timing jumper is moved to Timing position. The Phase signal becomes DClk delayed by 3 to 5 ns with the jumper in the Timing position.

‡ The Phase signal is normally DClk, but becomes IClk when caches are swapped. Setup time for IClk and DClk is 5 ns for clocking purposes, but 10 ns to generate the Phase signal.

§ MemRd*, MemWr*, Run*, and AccTyp(2:0) signals are sampled during the Data phase only; therefore, they are sampled by IClk when caches are not swapped and by DClk when caches are swapped.

¶ Exc* setup time is defined by the 92A96 Module specification. The probe adapter also latches the signal and uses it to decode a Fixup cycle; this requires a -0.1 ns minimum setup time.

\# Exc* hold time is defined by the latch on the probe adapter. If the delay from Clk2xSmp to Clk2XPhi is 6.5 ns or more, the 6.5 ns hold time requirement will be satisfied.

†† Exceeds R3000 requirements on inputs by 2.5 ns.

‡‡ Includes run capacitance and input capacitance of any integrated circuits (except the microprocessor) on the probe adapter and the input capacitance of the 92A96 probes.

§§ Includes dc impedance of any parts (except the microprocessor) on the probe adapter and the dc impedance of the 92A96 probes.

Table C-2
Physical Specifications

Characteristics	Description		
Overall Dimensions	Podlets Attached†		
(maximum) Probe Adapter		in	cm
Standard			
Length		3.80	≈ 9.65
Width		3.25	≈ 8.25
Height‡		2.24	≈ 5.69
Option 2S			
Length		7.50	≈ 19.05
Width		6.95	≈ 17.65
Height‡		1.18	≈ 3.01

Cable Length
    92A96 probe cable from the
    DAS 9200 to the tip of the
    8-channel probes
	5 ft 10.5 in ≈ 179 cm		

Weight	4.0.oz (113 g)		

† Excluding length of pins into SUT socket.
‡ With one socket extender and ZIF socket.

Table C-3
Environmental Specifications

Characteristic	Description

Temperature
  Max. Operating
  Min. Operating
  Non-Operating
	
	+50° C (+122° F)†
	+0° C (+32° F)
	-62° C to +85° C (-78° F to +185° F)

Humidity	10-95% relative humidity (non precipitating)

Altitude
  Operating
  Non-Operating
	
	15,000 ft. (4.5 km) maximum
	50,000 ft. (15 km) maximum

Electrostatic Immunity	The probe adapter is static-sensitive

† Not to exceed vendor's R3000/A thermal considerations. Cooling, using forced air,
  may be required across the CPU.

Table C-4 shows the 92A96 section and channel assignments, their grouping and default radix for the disassembler, the voltage threshold, polarity, and microprocessor signal and pin connections. In addition to the signals listed in the table are twelve signals not acquired by the 92A96 Module; these signals are listed in Table B-2.

Table C-4
92DM74 Channel Assignments

92DM74 Group (Radix)	Group Bit Pos	92A96 Section: Channel	Voltage Threshold, Polarity	R3000/A Signal Name	PGA
Address (Hex)	31	A3: 7	TTL, +	Tag31	L14
	30	A3: 6	TTL, +	Tag30	L15
	29	A3: 5	TTL, +	Tag29	J14
	28	A3: 4	TTL, +	Tag28	J13
	27	A3: 3	TTL, +	Tag27	K15
	26	A3: 2	TTL, +	Tag26	J15
	25	A3: 1	TTL, +	Tag25	H14
	24	A3: 0	TTL, +	Tag24	H15
	23	A2: 7	TTL, +	Tag23	F15
	22	A2: 6	TTL, +	Tag22	G14
	21	A2: 5	TTL, +	Tag21	F14
	20	A2: 4	TTL, +	Tag20	E14
	19	A2: 3	TTL, +	Tag19	D15
	18	A2: 2	TTL, +	Tag18	C15
	17	A2: 1	TTL, +	Tag17	D14
	16	A2: 0	TTL, +	Tag16	E13
	15	A1: 7	TTL, +	AdrLo15	A7
	14	A1: 6	TTL, +	AdrLo14	A6
	13	A1: 5	TTL, +	AdrLo13	B7
	12	A1: 4	TTL, +	AdrLo12	B5
	11	A1: 3	TTL, +	AdrLo11	A4
	10	A1: 2	TTL, +	AdrLo10	A3
	9	A1: 1	TTL, +	AdrLo9	B4
	8	A1: 0	TTL, +	AdrLo8	C5
	7	A0: 7	TTL, +	AdrLo7	B3
	6	A0: 6	TTL, +	AdrLo6	A2
	5	A0: 5	TTL, +	AdrLo5	C4
	4	A0: 4	TTL, +	AdrLo4	C2
	3	A0: 3	TTL, +	AdrLo3	B1
	2	A0: 2	TTL, +	AdrLo2	D2
	1	A0: 1	TTL, +	AdrLo1	E3
	0	A0: 0	TTL, +	AdrLo0	C1
Data (Hex)	31	D3: 7	TTL, +	Data31	Q4
	30	D3: 6	TTL, +	Data30	P8
	29	D3: 5	TTL, +	Data29	Q7
	28	D3: 4	TTL, +	Data28	Q5
	27	D3: 3	TTL, +	Data27	P6
	26	D3: 2	TTL, +	Data26	P5
	25	D3: 1	TTL, +	Data25	Q3
	24	D3: 0	TTL, +	Data24	N5
	23	D2: 7	TTL, +	Data23	P1
	22	D2: 6	TTL, +	Data22	P4
	21	D2: 5	TTL, +	Data21	Q2

(Cont.)

Table C-4 (Cont.)
92DM74 Channel Assignments

92DM74 Group (Radix)	Group Bit Pos	92A96 Section: Channel	Voltage Threshold, Polarity	R3000/A Signal Name	PGA
	20	D2: 4	TTL, +	Data20	P2
	19	D2: 3	TTL, +	Data19	N3
	18	D2: 2	TTL, +	Data18	N2
	17	D2: 1	TTL, +	Data17	L3
	16	D2: 0	TTL, +	Data16	M2
	15	D1: 7	TTL, +	Data15	K1
	14	D1: 6	TTL, +	Data14	N1
	13	D1: 5	TTL, +	Data13	M1
	12	D1: 4	TTL, +	Data12	L2
	11	D1: 3	TTL, +	Data11	K2
	10	D1: 2	TTL, +	Data10	J1
	9	D1: 1	TTL, +	Data9	J3
	8	D1: 0	TTL, +	Data8	H3
	7	D0: 7	TTL, +	Data7	F2
	6	D0: 6	TTL, +	Data6	H1
	5	D0: 5	TTL, +	Data5	H2
	4	D0: 4	TTL, +	Data4	G1
	3	D0: 3	TTL, +	Data3	G2
	2	D0: 2	TTL, +	Data2	F3
	1	D0: 1	TTL, +	Data1	D1
	0	D0: 0	TTL, +	Data0	E2
Control (Sym)	15	C2: 3	TTL, +	Run*,‡	N14
	14	C3: 2	TTL, +	Phase#	P11
	13	C2: 6	TTL, +	Exc*	Q8
	12	C2: 2	TTL, +	XEn*,‡	P7
	11	C3: 6	TTL, +	IRd*,‡	P12
	10	C3: 5	TTL, +	IWr*,†	P13
	9	C3: 4	TTL, +	DRd*,‡	N11
	8	C2: 5	TTL, +	DWr*,†	Q14
	7	C2: 1	TTL, +	MemRd*,‡	N13
	6	C2: 0	TTL, +	MemWr*,‡	N12
	5	C2: 4	TTL, +	RdBusy	C11
	4	C3: 0	TTL, +	WrBusy*	A13
	3	C3: 1	TTL, +	Reset*	A14
	2	C3: 7	TTL, +	AccTyp2	L13
	1	C3: 3	TTL, +	AccTyp1	M14
	0	C2: 7	TTL, +	AccTyp0	P15
Intr (Bin)	5	C0: 5	TTL, +	Int*(5)	A12
	4	C0: 4	TTL, +	Int*(4)	C10
	3	C0: 3	TTL, +	Int*(3)	B10
	2	C0: 2	TTL, +	Int*(2)	A11
	1	C0: 1	TTL, +	Int*(1)	B9
	0	C0: 0	TTL, +	Int*(0)	C9

(Cont.)

Table C-4 (Cont.)
92DM74 Channel Assignments

92DM74 Group (Radix)	Group Bit Pos	92A96 Section: Channel	Voltage Threshold, Polarity	R3000/A Signal Name	PGA
Misc	8	C1: 7	TTL, +	CPSync*	Q11
(Off)	7	C1: 1	TTL, +	BusError*	B12
	6	C0: 6	TTL, +	TagV	N15
	5	C1: 0	TTL, +	CpBusy	B11
	4	C0: 7	TTL, +	DRW_Fixup*=	§
	3	C1: 5	TTL, +	CpCond3 (AdrLo17)	A10
	2	C1: 4	TTL, +	CPCond2 (AdrLo16)	A9
	1	C1: 3	TTL, +	CPCond1	B8
	0	C1: 2	TTL, +	CpCond0	A8
Jumper (Off)	3	C1: 6	TTL, +	Endian	¶
Clock	3	CLK: 3	TTL, +	IClk	Q13
(not	2	CLK: 2	TTL, +	DClk	P11
stored)	1	CLK: 1	TTL, +	IRW_SC* (Synthesized)	††
	0	CLK: 0	TTL, +	DRW_Fixup* (Synthesized)	§

* Active low signals
† Buffered signals to guarantee Hold time for IWr* and DWr*.
‡ Latched signals to guarantee Hold time; buffered delay for these signals will not provide required Hold time.
§ DRW_Fixup*= is a synthesized signal which is the negative logical OR of the DRd*, DWr*, and Fixup* signals.
¶ The Endian signal is selected by the Big/Little-Endian jumper on the probe adapter.
# In Normal mode, the Phase signal identifies either an Instruction Phase (a logic high) or a Data Phase (logic low). The Phase signal is generated by selecting DClk when the caches are not swapped and IClk when the caches are swapped. It is always DClk when the Normal/Timing jumper is set to the Timing position.
†† IRW_SC* is a synthesized signal which is the negative logical OR of the IRd*, and IWr*signals and a signal that indicates the caches are swapped while the IClk signal is high

Figures C-1 and C-2 show the dimensions of the probe adapter with all the clock probes and 8-channel probes attached. Figure C-1 shows the standard probe adapter with straight square pins; Figures C-2 shows the option 2S probe adapter with 90°-bent square pins.
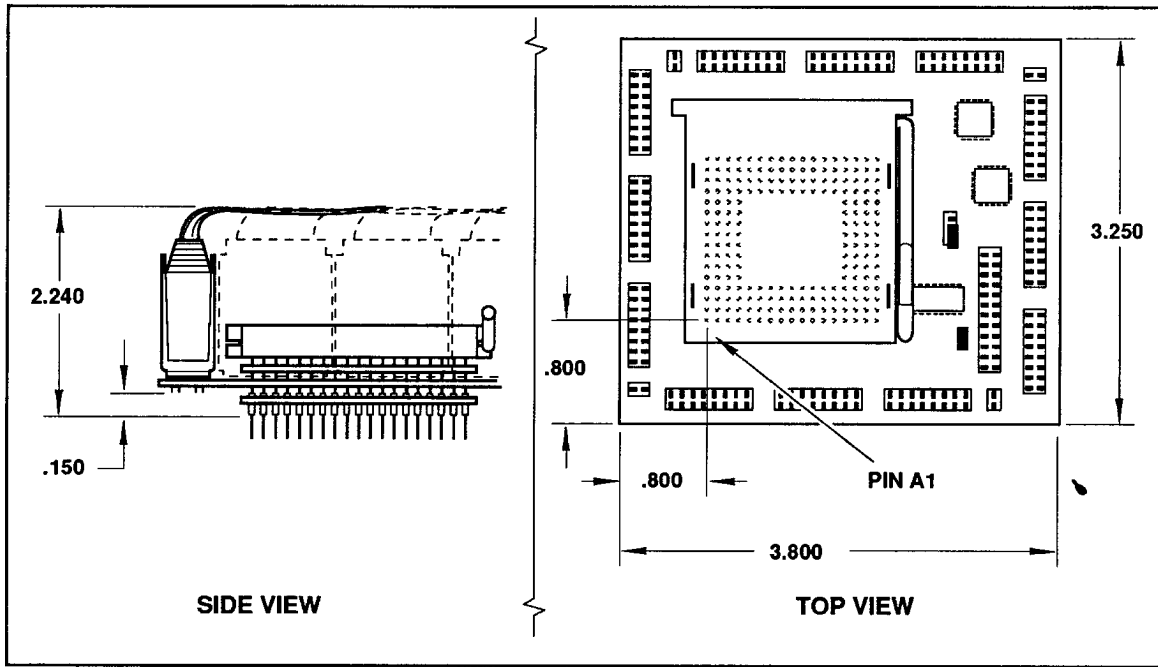
SIDE VIEW   TOP VIEW

Figure C-1. Minimum Clearance of the standard probe adapter with 8-channel probes attached.
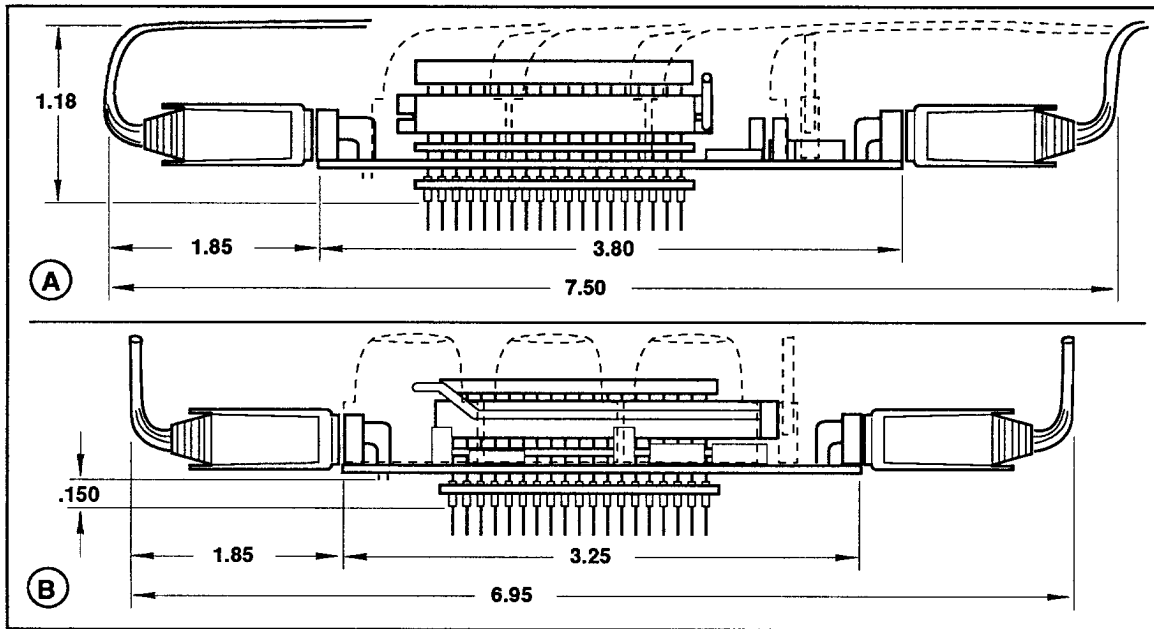

Figure C-2. Minimum Clearance of an optional 2S probe adapter with 8-channel probes attached.

DISCONNECTING CLOCK AND 8-CHANNEL PROBES

You may need to disconnect the clock and 8-channel probes from the probe adapter to use them on another application, to connect individual podlets to other signals in your R3000 system, or to replace defective clock or probe channels (podlets). Refer to Figure C-3 and the following procedure to disconnect the clock and 8-channel probes from the probe adapter. Use the antistatic shipping material to support the probe adapter while disconnecting the clock and 8-channel probes.
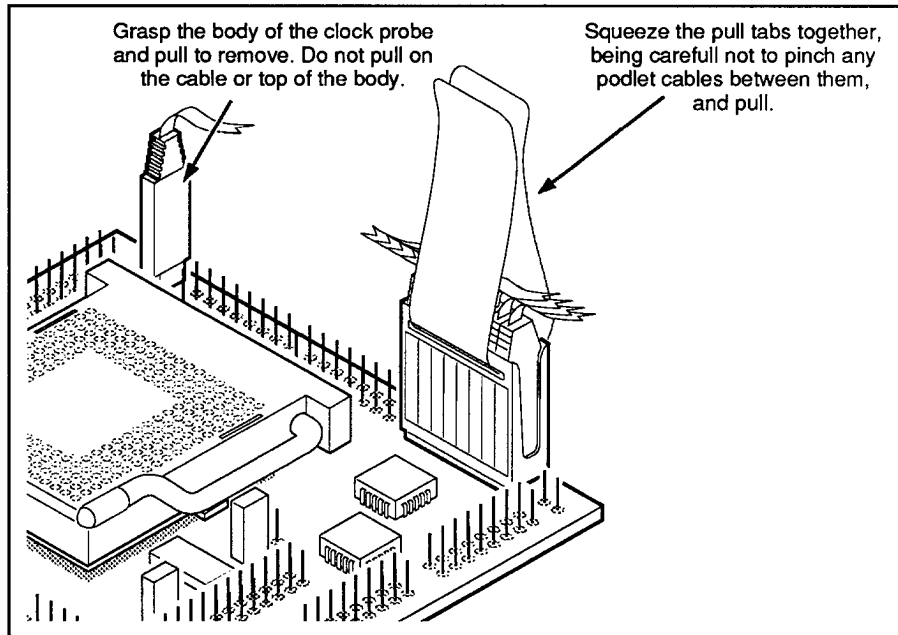
Figure C-3. Disconnecting clock and 8-channel probes.

1. Although not required, it is recommended that you power down the SUT; it is not necessary to power down the DAS 9200.

2. Firmly grasp the body of a clock probe and gently pull it off of the square pins.

{ *CAUTION* }

Pulling on the cables, on the neck of the clock probe, or pinching the cables between the pull tabs can damage the probe. Always handle the probes by their bodies.

3. Squeeze the pull tabs on the podlet holder together; be careful not to pinch any podlet cables between them.

4. Gently pull the 8-channel probe off of the square pins.

REMOVING AND REPLACING PODLETS

Each 8-channel probe consists of 8 single-channel podlets ganged together in a podlet holder. You may need to remove these podlets from the 8-channel probe to use for alternate connections to R3000 system signals.

Refer to the discussions on *Signals* in Appendix B and *Alternate Connections* in Section 3 for information about which channels you can use to make alternate connections between the DAS 9200 and system under test without disturbing the channel connections required for disassembly.

You can also use these procedures to replace a defective clock probe or a defective podlet from an 8-channel probe.

NOTE

> *The clock podlets and the 8-channel probe podlets are not interchangeable. Always replace a podlet with the appropriate type and channel color-coding.*

Removing a Clock Probe or 8-Channel Probe Podlet from the Interface Housing

Refer to Figure C-4 and the following procedure to remove a clock probe or an 8-channel probe podlet from the interface housing.

1. If necessary, disconnect the podlet from the probe adapter following the steps outlined in *Disconnecting Clock and 8-Channel Probes.*

2. Use a small pointed tool such as a ballpoint pen, pencil, or straightened paper clip to press down on the latch detent of the podlet through an opening on the interface housing.

3. Gently pull the podlet connector out of the housing with one hand while pressing down on the latch detent with the pointed tool.
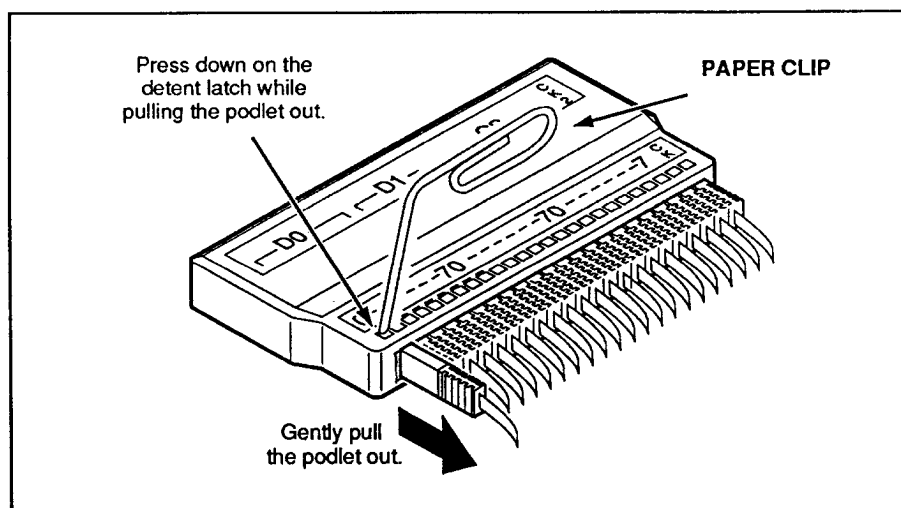
Figure C-4. Removing a clock or an 8-channel probe podlet from the interface housing.

Replacing a Clock Probe

Refer to Figure C-4 and the follow this procedure to replace a clock probe.

> To replace a clock probe, insert a new clock probe into the same clock channel position on the interface housing. Insert the clock probe into the interface housing with the detent latch oriented to the label side of the housing.

Removing 8-Channel Probe Podlets from the Podlet Holder

Refer to Figure C-5 and the following procedure to remove the 8-channel probe podlets from the podlet holder.

> ┌─────────────────┐
> │   CAUTION   │
> └─────────────────┘

Excessive pulling on the sides of the holder can damage the podlet holder: spread the holder open wide enough to clear and remove the podlets.

1. To remove podlets from the podlet holder, grasp the plastic pull tab on each side of the podlet holder and gently spread the sides of the holder open just enough to clear a podlet.

2. Remove the middle two podlets from the podlet holder by pushing up on the metal pin receptacles.

3. Release the tabs on the podlet holder.

4. Remove the remaining podlets by turning and extracting each one at a time.

CHANNEL 7
PODLET

CHANNEL 0
PODLET

Gently pull the tabs outward to open the podlet holder just enough to clear the two center podlets.

Figure C-5. Ganging together the 8-channel probe podlets.

Replacing 8-Channel Probe Podlets

The channel podlets must retain the same channel order on both the interface housing and in the podlet holder. Be sure to replace the old podlet with a podlet of the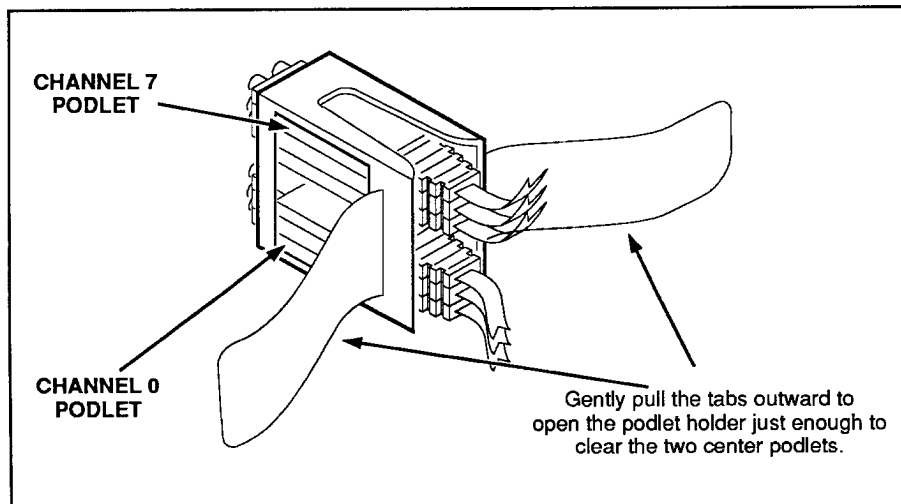 same color. Table C-5 shows the color code and channel number of each podlet for an 8-channel probe. Part numbers for the podlets are listed in the Replaceable Electrical Parts section of the *92A96 Service Manual* (070-7847-xx).

<div align="center">

Table C-5
Podlet-to-Channel Color Code

Podlet Color	Channel
Black	0
Brown	1
Red	2
Orange	3
Yellow	4
Green	5
Blue	6
Violet	7

</div>

Refer to Figure C-5 and the following procedure to replace an 8-channel probe podlet.

1. Insert the appropriately-colored podlet into the interface housing with the detent latch oriented to the label side of the housing.

2. If you are replacing a single podlet, orient the podlet connector marked GND towards the side of the podlet holder labeled GROUND.

3. Grasp the plastic pull tab on each side of the holder and gently spread the sides of the holder open just enough to clear the podlet.

4. Hold the podlet body with the other hand and place it in the holder in the correct channel order. Do not grasp and turn the podlet cable.

5. If you are re-grouping all the podlets of an 8-channel probe, begin grouping the podlets together starting with either channel 0 or channel 7. Orient the podlet channel marked GND towards the side of the podlet holder labeled GROUND.

<div align="center">

CAUTION

</div>

> *To prevent damage to the podlets, keep the podlet cables parallel to each other when grouping them into the holder. Avoid twisting the podlet cables between the interface housing and the podlet holder.*

6. Hold the podlet body, turn the podlet body parallel to the sides of the holder, move it into the holder, and use your fingers to press it into place perpendicular to the sides of the holder. Be sure to group the podlets in the correct channel order according to the channel label on the podlet holder and podlet color code, with all ground channels toward the Ground side of the holder. Do not place the podlet into the holder by grasping the podlet cable.

7. Continue placing the next two podlets, one at a time, in channel order, in the podlet holder. Orient all ground channels toward the Ground side of the holder.

8. The fourth podlet should be either channel 0 or 7, whichever one is not already placed in the holder. Place this podlet in the other end of the podlet holder and orient the ground channel correctly.

9. Continue placing the next two podlets, one at a time, in channel order, in the podlet holder. Continue orienting the ground channels correctly.

> *CAUTION*

Excessive pulling on the sides can break the podlet holder. Spread the holder open only wide enough to clear the podlet.

10. Grasp the plastic pull tab on each side of the holder and gently spread the sides of the holder open just enough to clear a podlet.

11. Place the last pair of podlets (channels 3 and 4) in the podlet holder in proper channel order, orienting the ground channels to the Ground side of the holder.

REMOVING AND REPLACING SOCKETS

The probe adapter board contains several sockets designed both to protect the probe adapter and to make it easy to insert and remove the R3000 microprocessor. Figure C-6 shows a side view of the board, sockets, and pins of the probe adapter. The fixed socket on top of the probe adapter board is soldered and cannot be removed. The following paragraphs describe how to remove and replace the ZIF socket and the protective socket on the bottom of the probe adapter board.
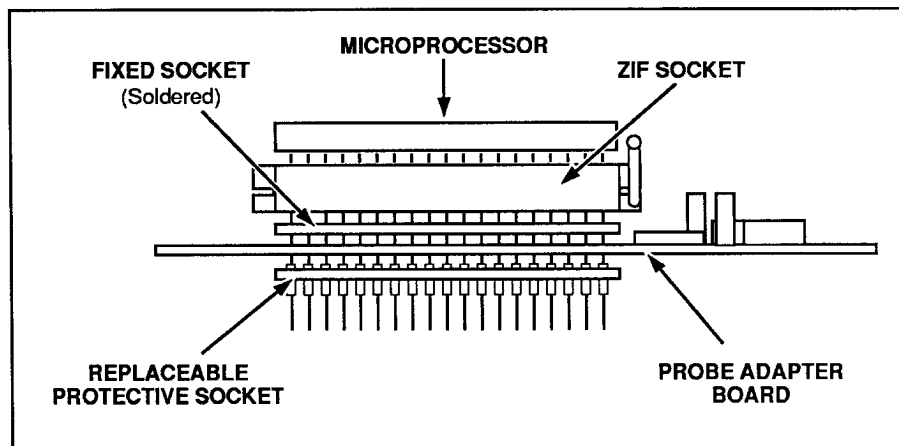
Figure C-6. Side view of the probe adapter board.

ZIF Socket

You should not have to remove the ZIF socket unless there are clearance problems, loading problems, or socket-pin damage. To remove the ZIF socket, refer to Figure C-6 and follow these steps:

1. Place a 3/16" flat-blade screwdriver between the fixed socket and the ZIF socket. The screwdriver should rest on the top of the body of the fixed socket.

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CAUTION
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Do not pry off one side of the ZIF socket and then the other. Applying uneven pressure can damage the ZIF socket's pins.

2. Apply even pressure around the entire socket by gently twisting the screwdriver against the body of the fixed socket and the ZIF socket until the ZIF socket is loose.

3. Remove the ZIF socket from the board.

4. Once the ZIF socket has been removed from the board, store the ZIF socket in protective foam so that the pins are not damaged.

To replace the ZIF socket, follow these steps:

1. Check that the ZIF socket's pins are straight.

2. Refer to Figure 2-3 or 3-5 for pin A1 location information.

3. After locating the correct pin A1 location, align the ZIF socket with the fixed socket on the board, making sure that all pins line up correctly.

4. Apply even pressure on the ZIF socket, so that all pins insert evenly.

Replaceable Protective Sockets

The R3000/A probe adapter is shipped with a 145-pin socket installed. If your system contains a 175-pin R3000A socket, you need to remove the protective socket shipped with the probe adapter and replace it with the 175-pin socket. To remove the protective socket, refer to Figure C-6 and follow these steps:

1. Locate the side of the socket adjacent to the edge of the probe adapter board and the side of the socket labeled A through S.

```
CAUTION
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Be careful not to damage any etched circuit board runs or components surrounding the protective socket when using a screwdriver to remove the protective socket from the bottom of the probe adapter board.

2. Place a 3/16" flat-blade screwdriver between the socket and the board on the side adjacent to the edge of the probe adapter board.

3. Gently twist the screwdriver against the body of the socket until the socket begins to separate from the probe adapter board pins.

CAUTION

Do not completely pry off one side of the protective socket and then the other. Applying uneven pressure can damage the socket's pins. Do not use board components as leverage to remove the socket.

4. Next, twist the screwdriver against the body of the socket next to the board marks A through S, but only where there are no board runs. Use even pressure alternately on both sides of the socket until the socket is loose.

5. Remove the socket from the board.

To replace the protective socket, follow these steps:

1. Check that the new socket's pins are straight.

2. Place the socket on the pins of the probe adapter board; make sure that all pins line up correctly and that the keying pin is properly located.

3. Press the socket onto the board by pressing it against a hard, flat surface while applying even pressure.

Replaceable Electrical Parts

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

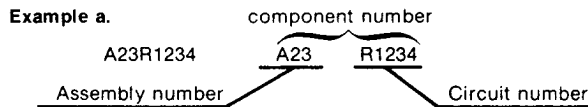### CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.
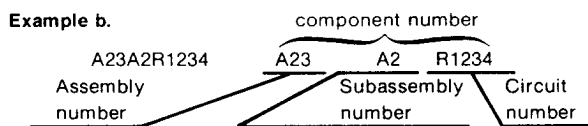
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.   component number

A23R1234   A23   R1234

Assembly number   Circuit number

Read: Resistor 1234 of Assembly 23

Example b.   component number

A23A2R1234   A23   A2   R1234

Assembly   Subassembly   Circuit
number   number   number

Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX – MFR CODE NUMBER TO MANUFACTURER

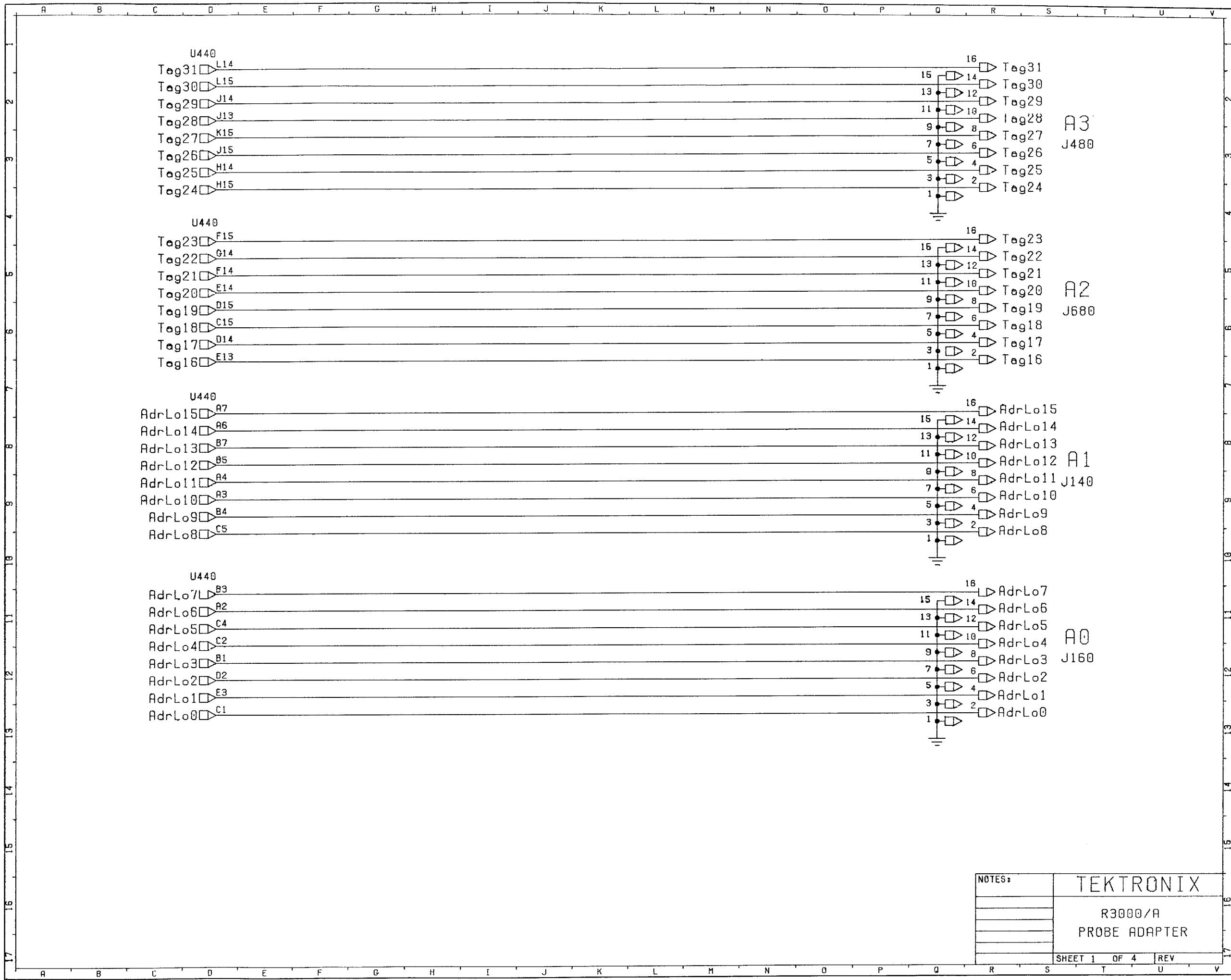| Mfr Code	Manufacturer	Address	City, State, Zip Code
04222	AVX CERAMICS DIV OF AVX CORP	19TH AVE SOUTH P O BOX 867	MYRTLE BEACH SC 29577
18324	SIGNETICS CORP	4130 S MARKET COURT	SACRAMENTO CA 95834-1222
22526	DU PONT E I DE NEMOURS AND CO INC	515 FISHING CREEK RD	NEW CUMBERLAND PA 17070-3007
53387	MINNESOTA MINING MFG CO	PO BOX 2963	AUSTIN TX 78769-2963
61772	INTEGRATED DEVICE TECHNOLOGY	3236 SCOTT BLVD	SANTA CLARA CA 95051
63058	MCKENZIE TECHNOLOGY	44370 OLD WARMS SPRINGS BLVD	FREMONT CA 94538
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR	BEAVERTON OR 97077-0001
91637	DALE ELECTRONICS INC	2064 12TH AVE	COLUMBUS NE 68601-3632
TK1462	YAMAICHI ELECTRONICS CO LTD 2ND FLOOR NEW KYOEI	3-CHROME SHIBAURA MINATO-KU	TOKYO JAPAN

REPLACEABLE ELECTRICAL PARTS

Component No.	Tektronix Part Number	Serial Number Effect	Serial Number Discont	Part Name & Description	Mfr Code	Mfr Part Number
A1	671-1978-00			CIRCUIT BD ASSY:92DM74,R3000/A TARGET HEAD (STANDARD ONLY)	80009	671-1978-00
A1	671-1979-00			CIRCUIT BD ASSY:92DM74;2S R3000/A TARGET (OPTION 2S,LOW PROFILE,ONLY)	80009	671-1979-00
A1	671-1978-00			CIRCUIT BD ASSY:92DM74,R3000/A TARGET HEAD (STANDARD ONLY)	80009	671-1978-00
A1	671-1979-00			CIRCUIT BD ASSY:92DM74;2S R3000/A TARGET (OPTION 2S,LOW PROFILE,ONLY)	80009	671-1979-00
A1C100	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	CC1206X7R104K050LR
A1C180	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	CC1206X7R104K050LR
A1C440	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	CC1206X7R104K050LR
A1C442	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	CC1206X7R104K050LR
A1C444	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	CC1206X7R104K050LR
A1C446	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	CC1206X7R104K050LR
A1C460	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	CC1206X7R104K050LR
A1C630	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	CC1206X7R104K050LR
A1C650	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	CC1206X7R104K050LR
A1C660	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	CC1206X7R104K050LR
A1C700	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	CC1206X7R104K050LR
A1C780	283-5004-00			CAP,FXD,CER DI:0.1UF,10%,25V	04222	CC1206X7R104K050LR
A1J120	131-5267-00			CONN,HDR:PCB,:MALE,STR,2 X 40,0.1 CTR,0.235 (STANDARD ONLY)	53387	2480-6122-TB
A1J120	131-5268-00			CONN,HDR:PCB,:MALE,RTANG,2 X 40,0.1 CTR (OPTION 2S,LOW PROFILE,ONLY)	53387	2480-5122-TB
A1J140	131-5267-00			CONN,HDR:PCB,:MALE,STR,2 X 40,0.1 CTR,0.235 (STANDARD ONLY)	53387	2480-6122-TB
A1J140	131-5268-00			CONN,HDR:PCB,:MALE,RTANG,2 X 40,0.1 CTR (OPTION 2S,LOW PROFILE,ONLY)	53387	2480-5122-TB
A1J160	131-5267-00			CONN,HDR:PCB,:MALE,STR,2 X 40,0.1 CTR,0.235 (STANDARD ONLY)	53387	2480-6122-TB
A1J160	131-5268-00			CONN,HDR:PCB,:MALE,RTANG,2 X 40,0.1 CTR (OPTION 2S,LOW PROFILE,ONLY)	53387	2480-5122-TB
A1J200	131-5267-00			CONN,HDR:PCB,:MALE,STR,2 X 40,0.1 CTR,0.235 (STANDARD ONLY)	53387	2480-6122-TB
A1J200	131-5268-00			CONN,HDR:PCB,:MALE,RTANG,2 X 40,0.1 CTR (OPTION 2S,LOW PROFILE,ONLY)	53387	2480-5122-TB
A1J280	131-5267-00			CONN,HDR:PCB,:MALE,STR,2 X 40,0.1 CTR,0.235 (STANDARD ONLY)	53387	2480-6122-TB
A1J280	131-5268-00			CONN,HDR:PCB,:MALE,RTANG,2 X 40,0.1 CTR (OPTION 2S,LOW PROFILE,ONLY)	53387	2480-5122-TB
A1J400	131-5267-00			CONN,HDR:PCB,:MALE,STR,2 X 40,0.1 CTR,0.235 (STANDARD ONLY)	53387	2480-6122-TB
A1J400	131-5268-00			CONN,HDR:PCB,:MALE,RTANG,2 X 40,0.1 CTR (OPTION 2S,LOW PROFILE,ONLY)	53387	2480-5122-TB
A1J480	131-5267-00			CONN,HDR:PCB,:MALE,STR,2 X 40,0.1 CTR,0.235 (STANDARD ONLY)	53387	2480-6122-TB
A1J480	131-5268-00			CONN,HDR:PCB,:MALE,RTANG,2 X 40,0.1 CTR (OPTION 2S,LOW PROFILE,ONLY)	53387	2480-5122-TB
A1J600	131-5267-00			CONN,HDR:PCB,:MALE,STR,2 X 40,0.1 CTR,0.235 (STANDARD ONLY)	53387	2480-6122-TB
A1J600	131-5268-00			CONN,HDR:PCB,:MALE,RTANG,2 X 40,0.1 CTR (OPTION 2S,LOW PROFILE,ONLY)	53387	2480-5122-TB
A1J620	131-0608-00			TERMINAL,PIN:PRESSFIT/PCB,:MALE,STR,0.025	22526	48283-036
A1J630	131-0608-00			TERMINAL,PIN:PRESSFIT/PCB,:MALE,STR,0.025	22526	48283-036
A1J640	131-0608-00			TERMINAL,PIN:PRESSFIT/PCB,:MALE,STR,0.025	22526	48283-036
A1J680	131-5267-00			CONN,HDR:PCB,:MALE,STR,2 X 40,0.1 CTR,0.235 (STANDARD ONLY)	53387	2480-6122-TB
A1J680	131-5268-00			CONN,HDR:PCB,:MALE,RTANG,2 X 40,0.1 CTR (OPTION 2S,LOW PROFILE,ONLY)	53387	2480-5122-TB

REPLACEABLE ELECTRICAL PARTS

Component No.	Tektronix Part Number	Serial Number Effect	Discont	Part Name & Description	Mfr Code	Mfr Part Number
A1J720	131-5267-00			CONN,HDR:PCB,:MALE,STR,2 X 40,0.1 CTR,0.235 (STANDARD ONLY)	53387	2480-6122-TB
A1J720	131-5268-00			CONN,HDR:PCB,:MALE,RTANG,2 X 40,0.1 CTR (OPTION 2S,LOW PROFILE,ONLY)	53387	2480-5122-TB
A1J740	131-5267-00			CONN,HDR:PCB,:MALE,STR,2 X 40,0.1 CTR,0.235 (STANDARD ONLY)	53387	2480-6122-TB
A1J740	131-5268-00			CONN,HDR:PCB,:MALE,RTANG,2 X 40,0.1 CTR (OPTION 2S,LOW PROFILE,ONLY)	53387	2480-5122-TB
A1J760	131-5267-00			CONN,HDR:PCB,:MALE,STR,2 X 40,0.1 CTR,0.235 (STANDARD ONLY)	53387	2480-6122-TB
A1J760	131-5268-00			CONN,HDR:PCB,:MALE,RTANG,2 X 40,0.1 CTR (OPTION 2S,LOW PROFILE,ONLY)	53387	2480-5122-TB
A1P620	131-0993-00			BUS,CONDUCTOR:SHUNT/SHORTING,:FEMALE,STR,1	22526	65474-006
A1P640	131-0993-00			BUS,CONDUCTOR:SHUNT/SHORTING,:FEMALE,STR,1	22526	65474-006
A1R640	321-5018-00			RES,FXD,FILM:1.00K,1%,0.125W	91637	CRCW12061001FT
A1R650	321-5042-00			RES,FXD,FILM:39.2 OHM,1%,0.125W	91637	CRCW120639R2FT
A1R651	321-5042-00			RES,FXD,FILM:39.2 OHM,1%,0.125W	91637	CRCW120639R2FT
A1U560	156-5908-00			IC,DIGITAL:FTTL,FLIP FLOP:DUAL D-TYPE,	18324	74F5074
A1U630	156-6275-00			IC,DIGITAL:FCTCMOS,LATCH:OCTAL D-TYPE,	61772	74FCT373CTSO
A1U650	160-8226-00			IC,DGTL:STTL,PLD:PRGM,16L8-5,PLCC20	80009	156622500
A1U660	160-8081-00			IC,DIGITAL:STTL,PLD:PRGM,16L8-5,PLCC20	80009	156622500

U440
Tag31 L14 — 16 Tag31
Tag30 L15 — 15 14 Tag30
Tag29 J14 — 13 12 Tag29
Tag28 J13 — 11 10 Tag28
Tag27 K15 — 9 8 Tag27
Tag26 J15 — 7 6 Tag26
Tag25 H14 — 5 4 Tag25
Tag24 H15 — 3 2 Tag24
1

A3
J480

U440
Tag23 F15 — 16 Tag23
Tag22 G14 — 15 14 Tag22
Tag21 F14 — 13 12 Tag21
Tag20 E14 — 11 10 Tag20
Tag19 D15 — 9 8 Tag19
Tag18 C15 — 7 6 Tag18
Tag17 D14 — 5 4 Tag17
Tag16 E13 — 3 2 Tag16
1

A2
J680

U440
AdrLo15 A7 — 16 AdrLo15
AdrLo14 A6 — 15 14 AdrLo14
AdrLo13 B7 — 13 12 AdrLo13
AdrLo12 B5 — 11 10 AdrLo12
AdrLo11 A4 — 9 8 AdrLo11
AdrLo10 A3 — 7 6 AdrLo10
AdrLo9 B4 — 5 4 AdrLo9
AdrLo8 C5 — 3 2 AdrLo8
1

A1
J140

U440
AdrLo7 B3 — 16 AdrLo7
AdrLo6 A2 — 15 14 AdrLo6
AdrLo5 C4 — 13 12 AdrLo5
AdrLo4 C2 — 11 10 AdrLo4
AdrLo3 B1 — 9 8 AdrLo3
AdrLo2 D2 — 7 6 AdrLo2
AdrLo1 E3 — 5 4 AdrLo1
AdrLo0 C1 — 3 2 AdrLo0
1

A0
J160

NOTES:

TEKTRONIX

R3000/A
PROBE ADAPTER

SHEET 1 OF 4   REV

U440

Data31 Q4 — 16 Data31
Data30 P8 — 15 14 Data30
Data29 Q7 — 13 12 Data29
Data28 Q5 — 11 10 Data28
Data27 P6 — 9 8 Data27
Data26 P5 — 7 6 Data26
Data25 Q3 — 5 4 Data25
Data24 N5 — 3 2 Data24
1

D3
J740

U440

Data23 P1 — 16 Data23
Data22 P4 — 15 14 Data22
Data21 Q2 — 13 12 Data21
Data20 P2 — 11 10 Data20
Data19 N3 — 9 8 Data19
Data18 N2 — 7 6 Data18
Data17 L3 — 5 4 Data17
Data16 M2 — 3 2 Data16
1

D2
J720

U440

Data15 K1 — 16 Data15
Data14 N1 — 15 14 Data14
Data13 M1 — 13 12 Data13
Data12 L2 — 11 10 Data12
Data11 K2 — 9 8 Data11
Data10 J1 — 7 6 Data10
Data9 J3 — 5 4 Data9
Data8 H3 — 3 2 Data8
1

D1
J400

U440

Data7 F2 — 16 Data7
Data6 H1 — 15 14 Data6
Data5 H2 — 13 12 Data5
Data4 G1 — 11 10 Data4
Data3 G2 — 9 8 Data3
Data2 F3 — 7 6 Data2
Data1 D1 — 5 4 Data1
Data0 E2 — 3 2 Data0
1

D0
J200

NOTES:

TEKTRONIX

R3000/A
PROBE ADAPTER

SHEET 2 OF 4   REV

ICLK — IClk CK3

U440
AccTyp(2) L13 — AccTyp(2) C3
L_IRd* — L_IRd*
B_IWr* — B_IWr* J760
L_DRd* — L_DRd*
AccTyp(1) M14 — AccTyp(1)
U440
Phase — Phase
Reset* A14 — Reset*
WrBusy* A13 — WrBusy*
U440

DClk — DClk CK2

U440
AccTyp(0) P15 — AccTyp(0)
Exc* — Exc*
B_DWr* — B_DWr*
RdBusy C11 — RdBusy C2
U440
L_Run* — L_Run* J600
L_XEn* — L_XEn*
L_MemRd* — L_MemRd*
L_MemWr* — L_MemWr*

IRW_SC* —

CpSync* P14
U440

VCC1
LITTLE
J640
ENDIAN — IRW_SC* CK1
BIG
CpSync*
Endian — Endian
CpCond(3) A10 — CpCond(3)
CpCond(2) A9 — CpCond(2) C1
CpCond(1) B8 — CpCond(1)
CpCond(0) A8 — CpCond(0) J280
BusError* B12 — BusError*
CpBusy B11 — CpBusy
U440

DRW_Fixup* — DRW_Fixup* CK0

DRW_Fixup*
TagV N15 — TagV C0
Int*(5) A12 — Int*(5)
Int*(4) C10 — Int*(4) J120
Int*(3) B10 — Int*(3)
Int*(2) A11 — Int*(2)
Int*(1) B9 — Int*(1)
Int*(0) C9 — Int*(0)
U440

NOTES:

TEKTRONIX

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PROBE ADAPTER

SHEET 3 OF 4 REV

TEKTRONIX

Rev A 11/01/90

R3000/A
PROBE ADAPTER

SHEET 4 OF 4   REV A

Replaceable Mechanical Parts

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5   Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
               ···· END ATTACHING PARTS ····
   Detail Part of Assembly and/or Component
   Attaching parts for Detail Part
               ···· END ATTACHING PARTS ····
   Parts of Detail Part
   Attaching parts for Parts of Detail Part
               ···· END ATTACHING PARTS ····

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - · - - - indicates the end of attaching parts.

ABBREVIATIONS

"	INCH	ELCTRN	ELECTRON	IN	INCH	SE	SINGLE END
#	NUMBER SIZE	ELEC	ELECTRICAL	INCAND	INCANDESCENT	SECT	SECTION
ACTR	ACTUATOR	ELCTLT	ELECTROLYTIC	INSUL	INSULATOR	SEMICOND	SEMICONDUCTOR
ADPTR	ADAPTER	ELEM	ELEMENT	INTL	INTERNAL	SHLD	SHIELD
ALIGN	ALIGNMENT	EPL	ELECTRICAL PARTS LIST	LPHLDR	LAMPHOLDER	SHLDR	SHOULDERED
AL	ALUMINUM	EQPT	EQUIPMENT	MACH	MACHINE	SKT	SOCKET
ASSEM	ASSEMBLED	EXT	EXTERNAL	MECH	MECHANICAL	SL	SLIDE
ASSY	ASSEMBLY	FIL	FILLISTER HEAD	MTG	MOUNTING	SLFLKG	SELF-LOCKING
ATTEN	ATTENUATOR	FLEX	FLEXIBLE	NIP	NIPPLE	SLVG	SLEEVING
AWG	AMERICAN WIRE GAGE	FLH	FLAT HEAD	NON WIRE	NOT WIRE WOUND	SPR	SPRING
BD	BOARD	FLTR	FILTER	OBD	ORDER BY DESCRIPTION	SQ	SQUARE
BRKT	BRACKET	FR	FRAME or FRONT	OD	OUTSIDE DIAMETER	SST	STAINLESS STEEL
BRS	BRASS	FSTNR	FASTENER	OVH	OVAL HEAD	STL	STEEL
BRZ	BRONZE	FT	FOOT	PH BRZ	PHOSPHOR BRONZE	SW	SWITCH
BSHG	BUSHING	FXD	FIXED	PL	PLAIN or PLATE	T	TUBE
CAB	CABINET	GSKT	GASKET	PLSTC	PLASTIC	TERM	TERMINAL
CAP	CAPACITOR	HDL	HANDLE	PN	PART NUMBER	THD	THREAD
CER	CERAMIC	HEX	HEXAGON	PNH	PAN HEAD	THK	THICK
CHAS	CHASSIS	HEX HD	HEXAGONAL HEAD	PWR	POWER	TNSN	TENSION
CKT	CIRCUIT	HEX SOC	HEXAGONAL SOCKET	RCPT	RECEPTACLE	TPG	TAPPING
COMP	COMPOSITION	HLCPS	HELICAL COMPRESSION	RES	RESISTOR	TRH	TRUSS HEAD
CONN	CONNECTOR	HLEXT	HELICAL EXTENSION	RGD	RIGID	V	VOLTAGE
COV	COVER	HV	HIGH VOLTAGE	RLF	RELIEF	VAR	VARIABLE
CPLG	COUPLING	IC	INTEGRATED CIRCUIT	RTNR	RETAINER	W/	WITH
CRT	CATHODE RAY TUBE	ID	INSIDE DIAMETER	SCH	SOCKET HEAD	WSHR	WASHER
DEG	DEGREE	IDENT	IDENTIFICATION	SCOPE	OSCILLOSCOPE	XFMR	TRANSFORMER
DWR	DRAWER	IMPLR	IMPELLER	SCR	SCREW	XSTR	TRANSISTOR

CROSS INDEX – MFR CODE NUMBER TO MANUFACTURER

Mfr Code	Manufacturer	Address	City, State, Zip Code
22526	DU PONT E I DE NEMOURS AND CO INC	515 FISHING CREEK RD	NEW CUMBERLAND PA 17070-3007
53387	MINNESOTA MINING MFG CO	PO BOX 2963	AUSTIN TX 78769-2963
63058	MCKENZIE TECHNOLOGY	44370 OLD WARMS SPRINGS BLVD	FREMONT CA 94538
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR	BEAVERTON OR 97077-0001
TK1462	YAMAICHI ELECTRONICS CO LTD 2ND FLOOR NEW KYOEI	3-CHROME SHIBAURA MINATO-KU	TOKYO JAPAN

REPLACEABLE MECHANICAL PARTS

Fig. & Index No.	Tektronix Part Number	Serial Number Effect	Serial Number Discont	Qty	12345 Part Name & Description	Mfr Code	Mfr Part Number
C7 -	010-0516-00			1	ADAPTER,PROBE:92DM74,R3000/A PGA (STANDARD ONLY)	80009	010-0516-00
	010-0517-00			1	ADAPTER,PROBE:92DM74:2S,R3000/A PGA 144/175 (OPTION 2S,LOW PROFILE,ONLY)	80009	010-0517-00
-1	136-0954-00			1	.SKT,PL-IN ELEK:PGA,ZIF:15 X 15 176 PIN	TK1462	NP35-18022-G42AF-176
-2	671-1978-00			1	.CIRCUIT BD ASSY:92DM74,R3000/A TARGET HEAD (STANDARD ONLY)	80009	671-1978-00
	671-1979-00			1	.CIRCUIT BD ASSY:92DM74:2S R3000/A TARGET (OPTION 2S,LOW PROFILE,ONLY)	80009	671-1979-00
-3	----- -----			1	..SKT,PL-IN ELEK:PGA,176 PIN,15 X 15,LONG (NOT REPLACEABLE;ORDER 671-1978-00 FOR		
-4	131-0608-00			30	..TERMINAL,PIN:PRESSFIT/PCB.:MALE,STR,0.025	22526	48283-036
-5	131-0993-00			2	BUS,CONDUCTOR:SHUNT/SHORTING,;FEMALE,STR,1	22526	65474-006
-6	131-5267-00			3	..CONN,HDR:PCB,:MALE,STR,2 X 40,0.1 CTR,0.2 (USED ON 671-1978-00)	53387	2480-6122-TB
-7	131-5268-00			3	..CONN,HDR:PCB,:MALE,RTANG,2 X 40,0.1 CTR (OPTION 2S,LOW PROFILE,ONLY)	53387	2480-5122-TB
-8	136-0952-00			2	.SKT,PL-IN ELEK:PGA,145 PIN,15 X 15,SHORT (FOR USE WITH R3000)	63058	PGA145H101B11521F
	136-1140-00			2	.SKT,PL-IN ELEK:PGA,175 PIN,15 X 15 (SHORTT (FOR USE WITH R3000A)	63058	PGA175H101B1 15A5F

STANDARD ACCESSORY

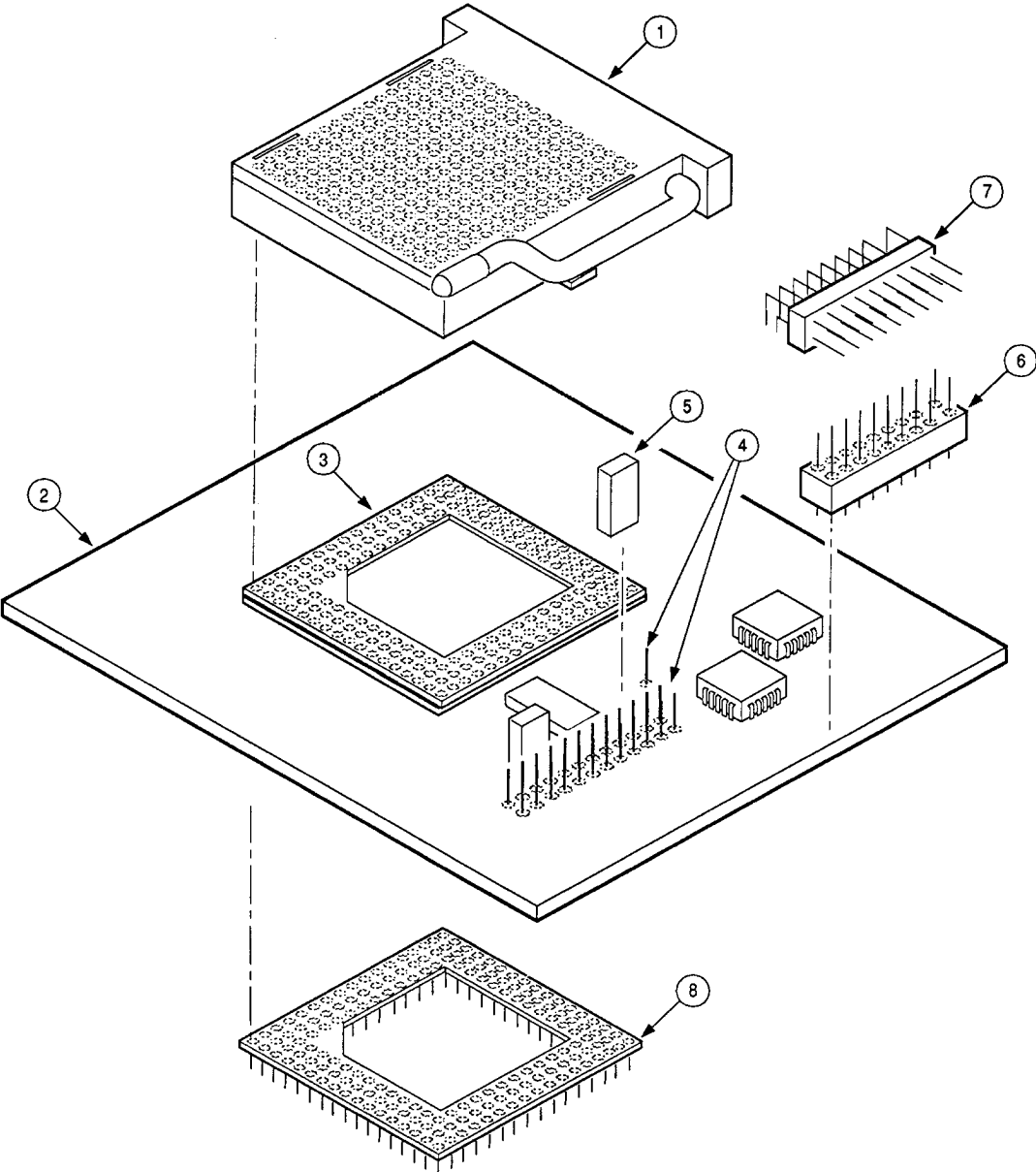| Fig. & Index No.	Tektronix Part Number	Serial Number Effect	Serial Number Discont	Qty	12345 Part Name & Description	Mfr Code	Mfr Part Number
	070-8090-00			1	MANUAL,TECH:INSTRUCTION,92DM74	80009	070-8090-00

Figure C-7. Probe adapter exploded view.

DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

SYMBOLS

Graphic symbol and class designation letters are based on ANSI Y32.14, 1973 in terms of positive logic. Logic symbols are depicted according to the manufacturer's data book information (not according to function).

Letter symbols for quantities used in electrical science and electrical engineering are based on ANSI Y10.5, 1968.

Drafting practices, line conventions, and lettering conform to ANSI Y14.15, 1966 and ANSI Y14.2, 1973.

Abbreviations are based on ANSI Y1.1, 1972.

You can inquire about these ANSI standards by contacting:

American National Standard Institute
1430 Broadway
New York, New York 10018

COMPONENT VALUES

Electrical components shown on the diagram are in the following units unless noted otherwise:
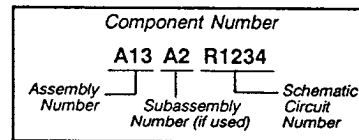
Capacitors = Values one or greater are in picofarads(pF)
Values less then one are in microfarads (μF)

Resistors = Ohms (Ω)

ACTIVE-LOW SIGNAL INDICATORS

A common convention used for indicating an active-low signal (a signal performing its intended function when it is in a low state) is an overbar, as shown in the signal name $\overline{\text{RESET}}$. The overbar may be used in this manual whenever a reference is given to an active-low signal. However, the same active-low signal is indicated on the schematic with a tilde ($\sim$), or a slash (/) following the signal name (e.g., RESET$\sim$ or RESET/).

The information and special symbols below may appear in this manual.

ASSEMBLY NUMBERS

Each assembly in the instrument is assigned an assembly number (e.g., A5). The assembly number appears in the title of each:

- schematic diagram (lower right corner)
- circuit board component location illustration
- schematic or circuit board component location look up table (when shown).

The Replaceable Electrical Parts list is arranged by assemblies in numerical order. The components are listed alphabetically by component location numbers. Look at the following example to see how to construct a component number.

COMPONENT NUMBER EXAMPLE

Component Number

A13 A2 R1234

Assembly Number — Subassembly Number (if used) — Schematic Circuit Number

Chassis mounted components have no Assembly Number prefix – see end of Replaceable Parts List.

GRID COORDINATES

The schematic diagram(s) and circuit board component location illustration both have grids. A look up table (when shown) provides grid coordinates for ease of locating components. There may be two tables for each assembly: one for the circuit board component location illustration and one for the schematic diagram(s).
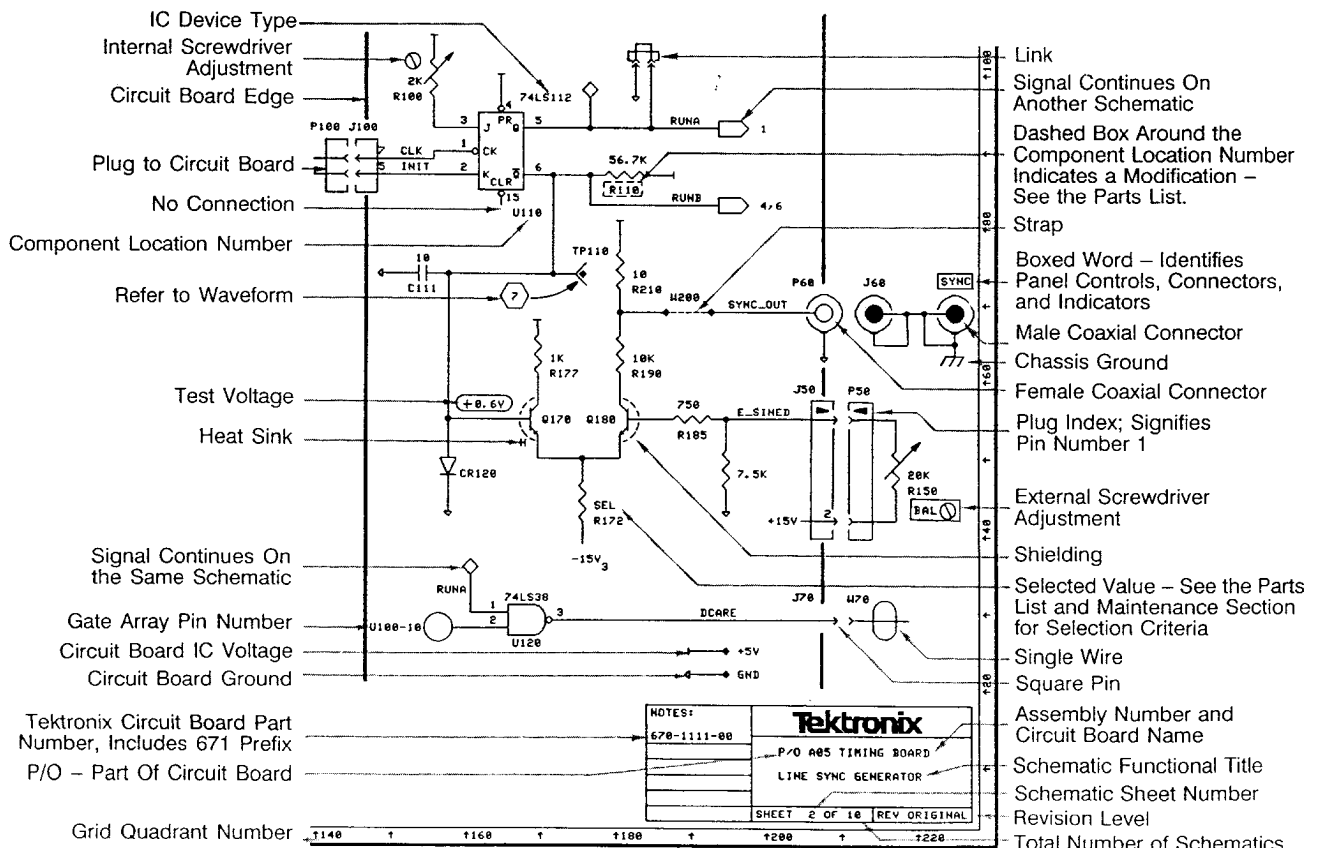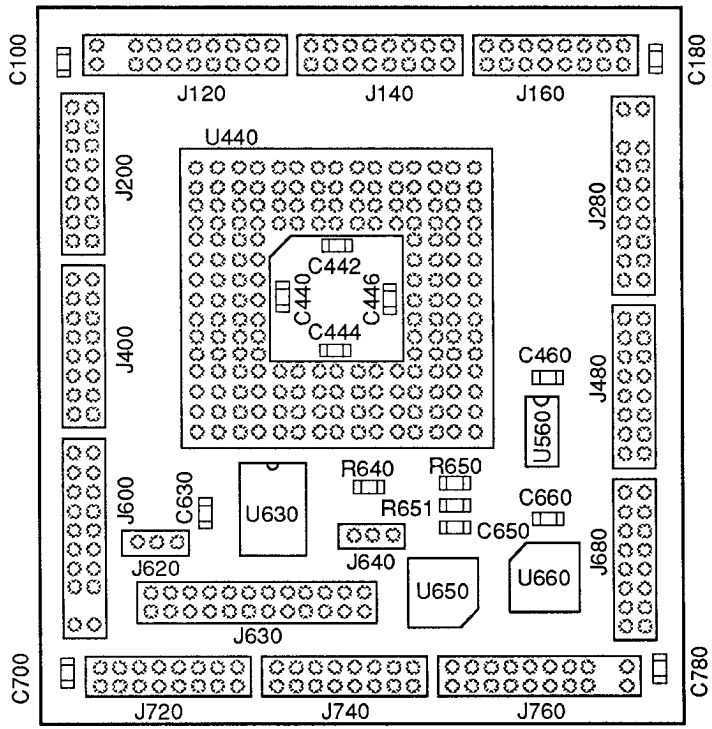
92DM74 Probe Adapter board component locations.